

MODEL NAME : *DDK51 - Firestar MLK / DDK52 - Firestar-B / DDK53 - Armani MLK*

PCB NO : *LA-E993P*

BOM P/N : *Firestar MLK/Firestar-B* *Armani MLK:*

- 451A9U31L01

451A9U31L02

451A9U31L03

451A9U31L04
- 451A9U31L51

451A9U31L52

451A9U31L53

451A9U31L54

Dell/Compal Confidential

Schematic Document

Coffee Lake-H

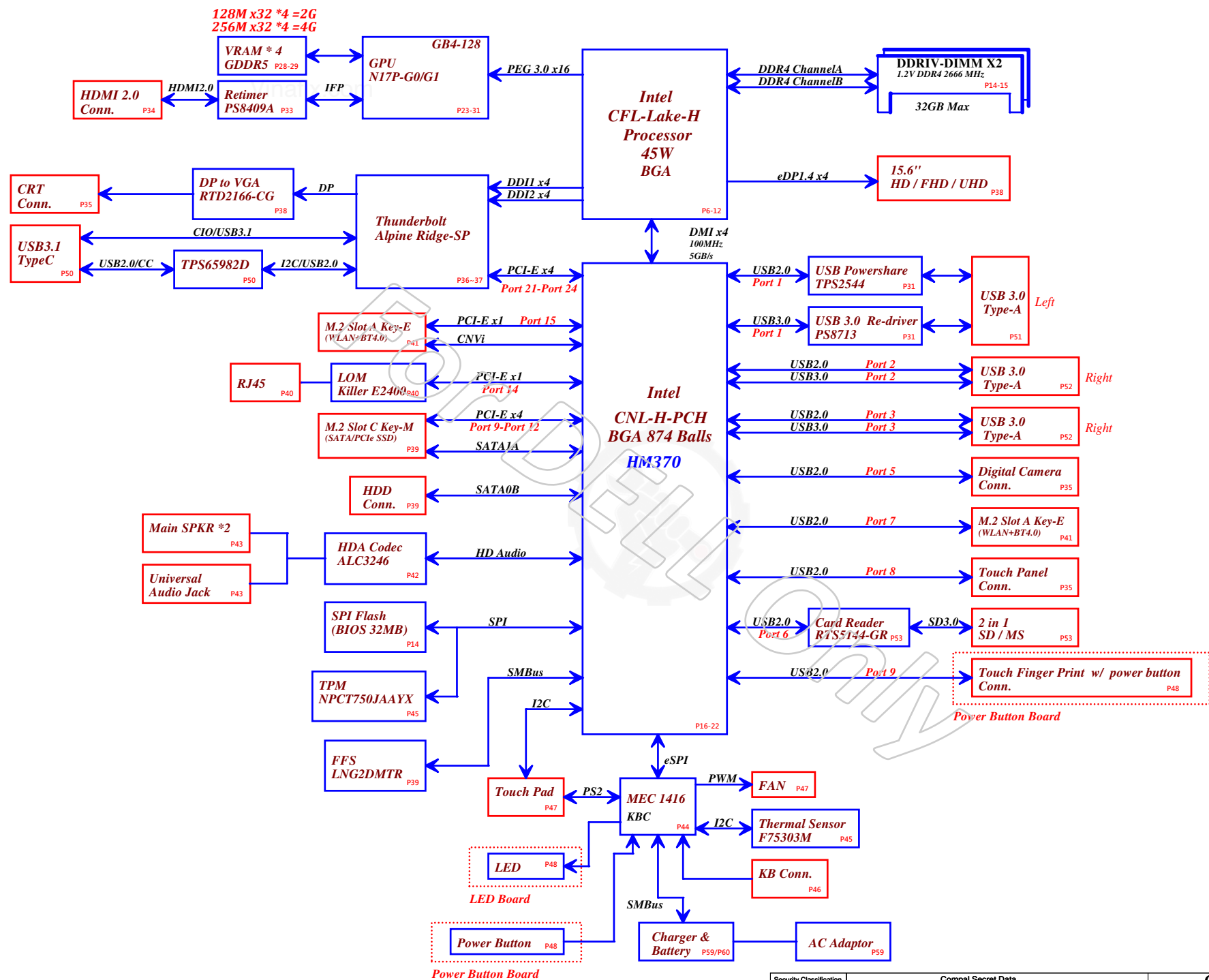
N17P

Firestar-B, Firestar/Armani MLK

2018-03-06

Rev: 1.0 (A00)

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				Rev	1.0(A00)



Board ID	Resistor
X00	10K
X01	17.8K
X02	27K
X03	37.4K
A00	49.9K

USB3	DESTINATION
1	USB JUSB3 (Left Side)
2	USB JUSB1 (Right Side)
3	USB JUSB2 (Right Side)
4	None
5	None
6	None

USB2	DESTINATION
1	USB JUSB3 (Left Side)
2	USB JUSB1 (Right Side)
3	USB JUSB2 (Right Side)
4	None
5	CAMERA
6	Card Reader
7	NGFF - WLAN + BT
8	Touch screen
9	Finger Print
10	None
11	None
12	None
13	None
14	None

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	None	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9			
Lane 10	NGFF - NVMe SSD	SATA	DESTINATION
Lane 11		0a	None (NVMe)
Lane 12		1a	NGFF - SSD
Lane 13	None (HDD)	0b	HDD
Lane 14	LOM	1b	None (LOM)
Lane 15	NGFF - WLAN	2	None (WLAN)
Lane 16	None	3	None
Lane 17		4	None
Lane 18		5	None
Lane 19			
Lane 20			
Lane 21			
Lane 22	Alpine Ridge - SP		
Lane 23			
Lane 24			

Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

13.2.1 Coffee Lake PCH-H

Figure 13-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support	No Support						No Support						Yes				No Support				Yes				Yes					

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

CLK_PCIE	DESTINATION	CLK_REQ	DESTINATION
0	None	0	None
1	None	1	None
2	LOM	2	LOM
3	NGFF - WLAN + BT	3	NGFF - WLAN + BT
4	None	4	None
5	Alpine Ridge - SP	5	Alpine Ridge - SP
6	NGFF - SSD	6	NGFF - SSD
7	GPU	7	GPU
8	None	8	None
9	None	9	None
10	None	10	None
11	None	11	None
12	None	12	None
13	None	13	None
14	None	14	None
15	None	15	None

eSPI Virtual Wires (VW) (Sheet 1 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SUS_STAT#	Output	ESPI_RESET#	No
SUS_PWRDN_ACK	Output	ESPI_RESET#	No
PLTRST#	Output	ESPI_RESET#	Yes
PME#	Input	ESPI_RESET#	No
WAKE#	Input	ESPI_RESET#	No
SMI#	Input	PLTRST#	N/A
SCI#	Input	PLTRST#	N/A
RCIN#	Input	PLTRST#	No
SLP_A#	Output	ESPI_RESET#	Yes

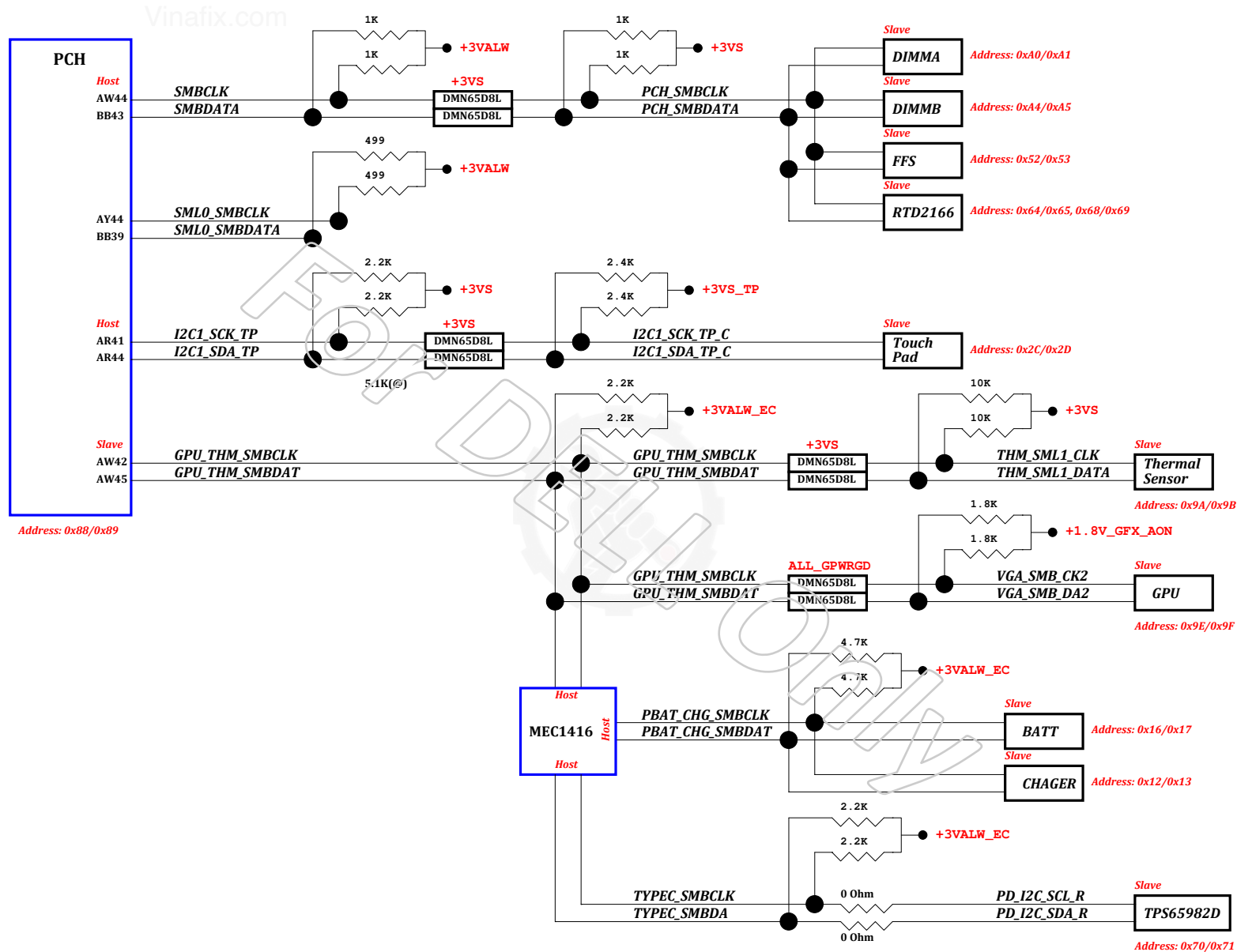
eSPI Virtual Wires (VW) (Sheet 2 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SLP_S3#/SLP_S4#/ SLP_S5#/SLP_LAN#/ SLP_WLAN#	Output	DSW_PWROK	Yes

Symbol Note :

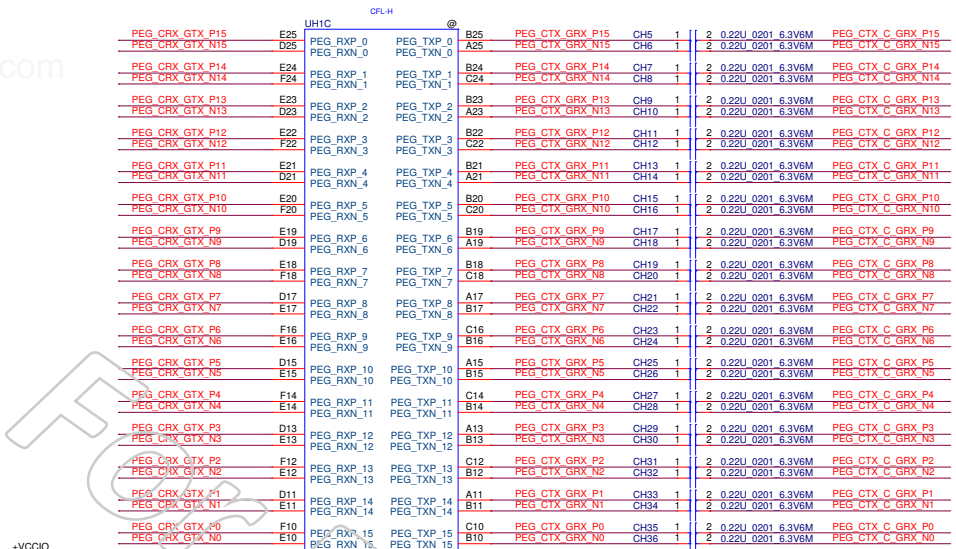
↓ : means Digital Ground

⏏ : means Analog Ground



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<23> PEG_CTX_C_GRX_P[0..15] PEG_CTX_C_GRX_P[0..15]
<23> PEG_CTX_C_GRX_N[0..15] PEG_CTX_C_GRX_N[0..15]
<23> PEG_CRX_GTX_P[0..15] PEG_CRX_GTX_P[0..15]
<23> PEG_CRX_GTX_N[0..15] PEG_CRX_GTX_N[0..15]

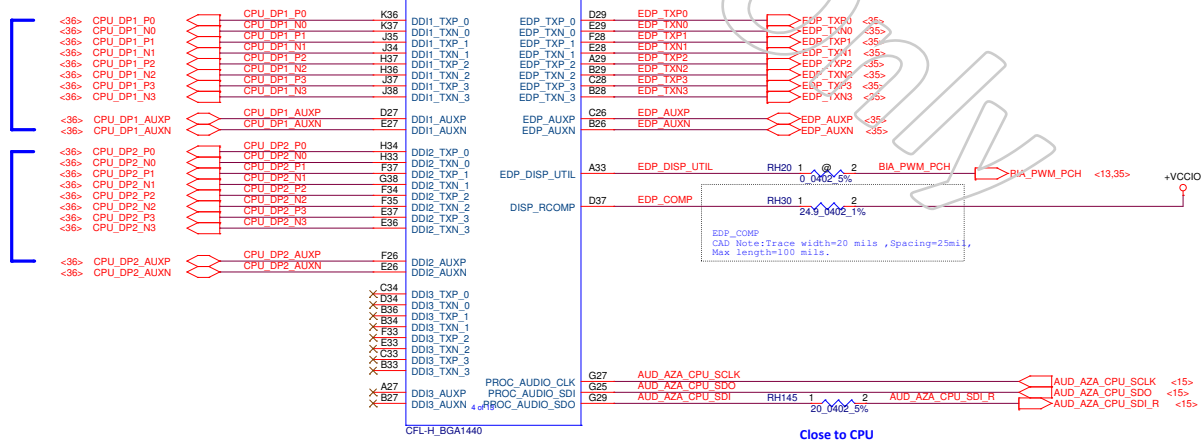


To PCH

To PCH

TBT-AR

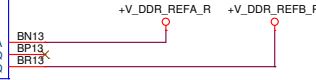
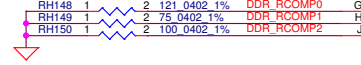
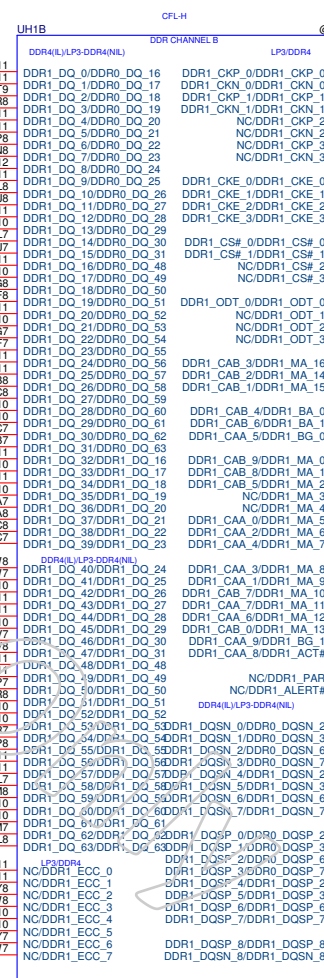
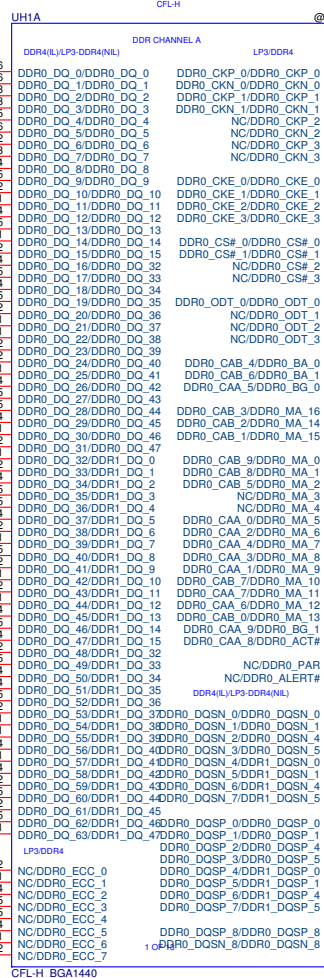
TBT-AR



Close to CPU

Non-Interleave

Vinafix.com



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								Document Number		
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								Sheet 7 of 78		

CFG Straps for Processor

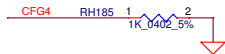
Stall reset sequence after CPU PLL lock until de-asserted	
CFG0	<p>★ 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>★ 0: Lane Reversed</p>



Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

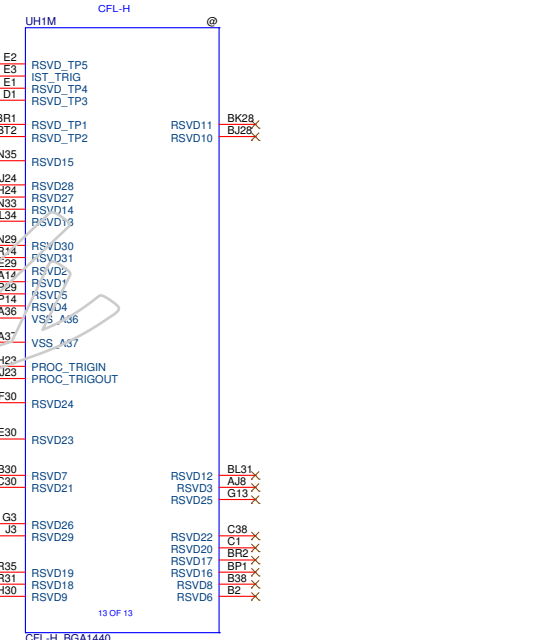
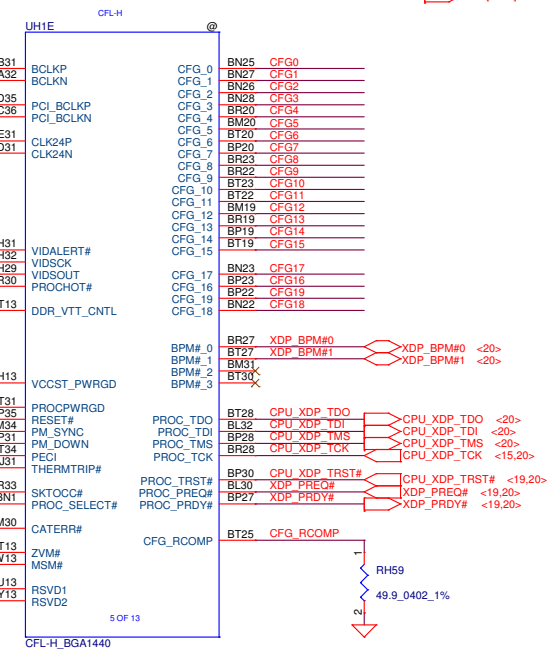
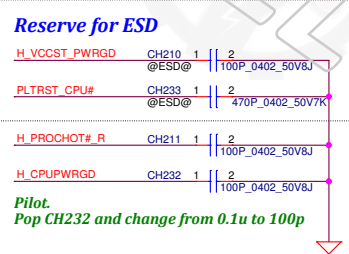
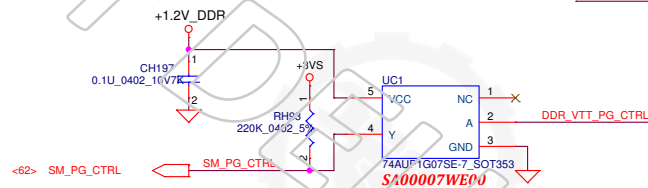
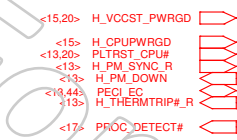
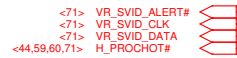
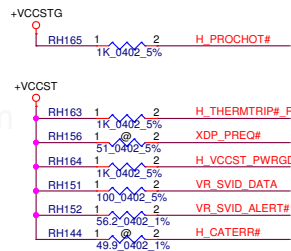


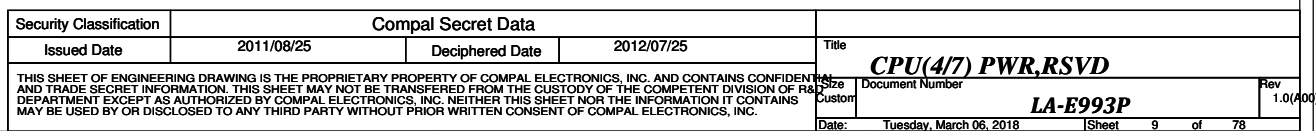
PCIe Port Bifurcation Straps	
CFG[6:5]	<p>★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>



If change to x8, need change setting.

PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



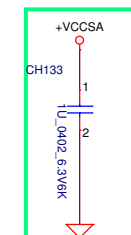
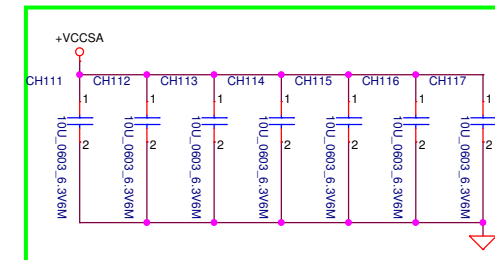
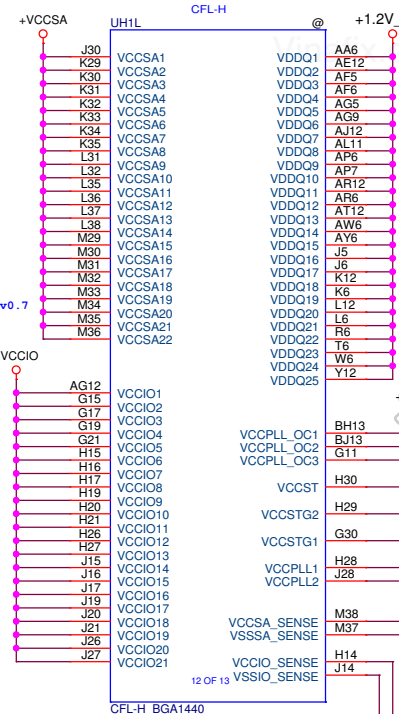


570805_CFL_EDS_Vol1_Rev0.7

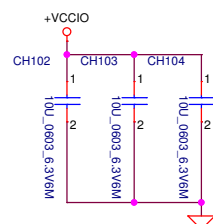
+VCC_SA
Max: 11100mA

570805_CFL_EDS_Vol1_Rev0.7

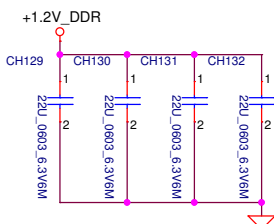
+VCC_IO
Max: 6400mA



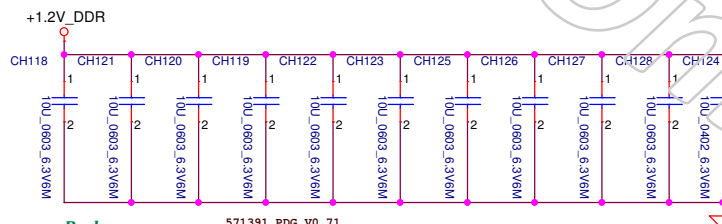
DVT2.
Add CH234 22uF 0603 cap
close to CPU Ball H30/J28



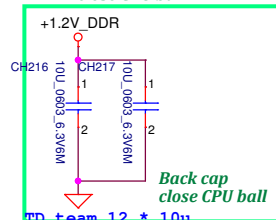
Back cap
close CPU ball



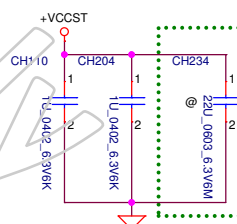
Back cap
close CPU ball



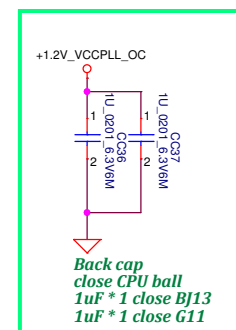
Back cap
close CPU ball



Back cap
close CPU ball



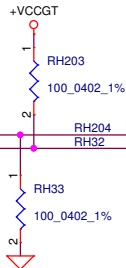
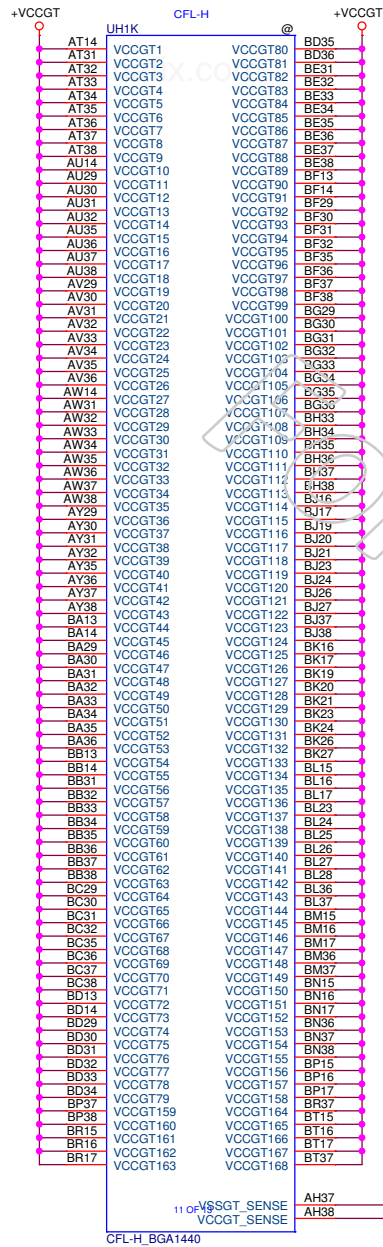
Back cap
close CPU ball
1uF * 1 close H30
1uF * 1 close J28



Back cap
close CPU ball
1uF * 1 close B/J13
1uF * 1 close G11

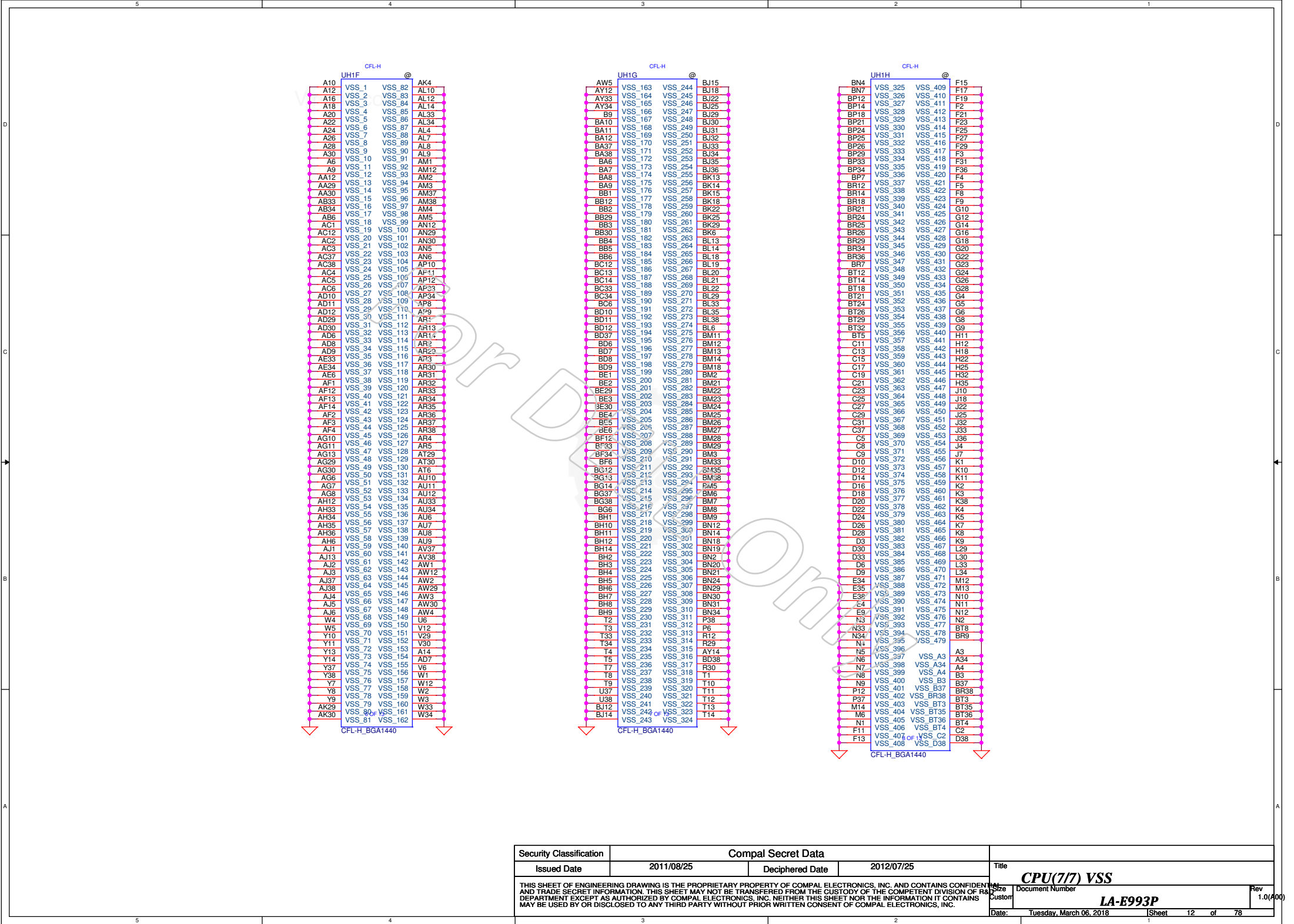
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GT
55000mA(Hexa Core GT2)



1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

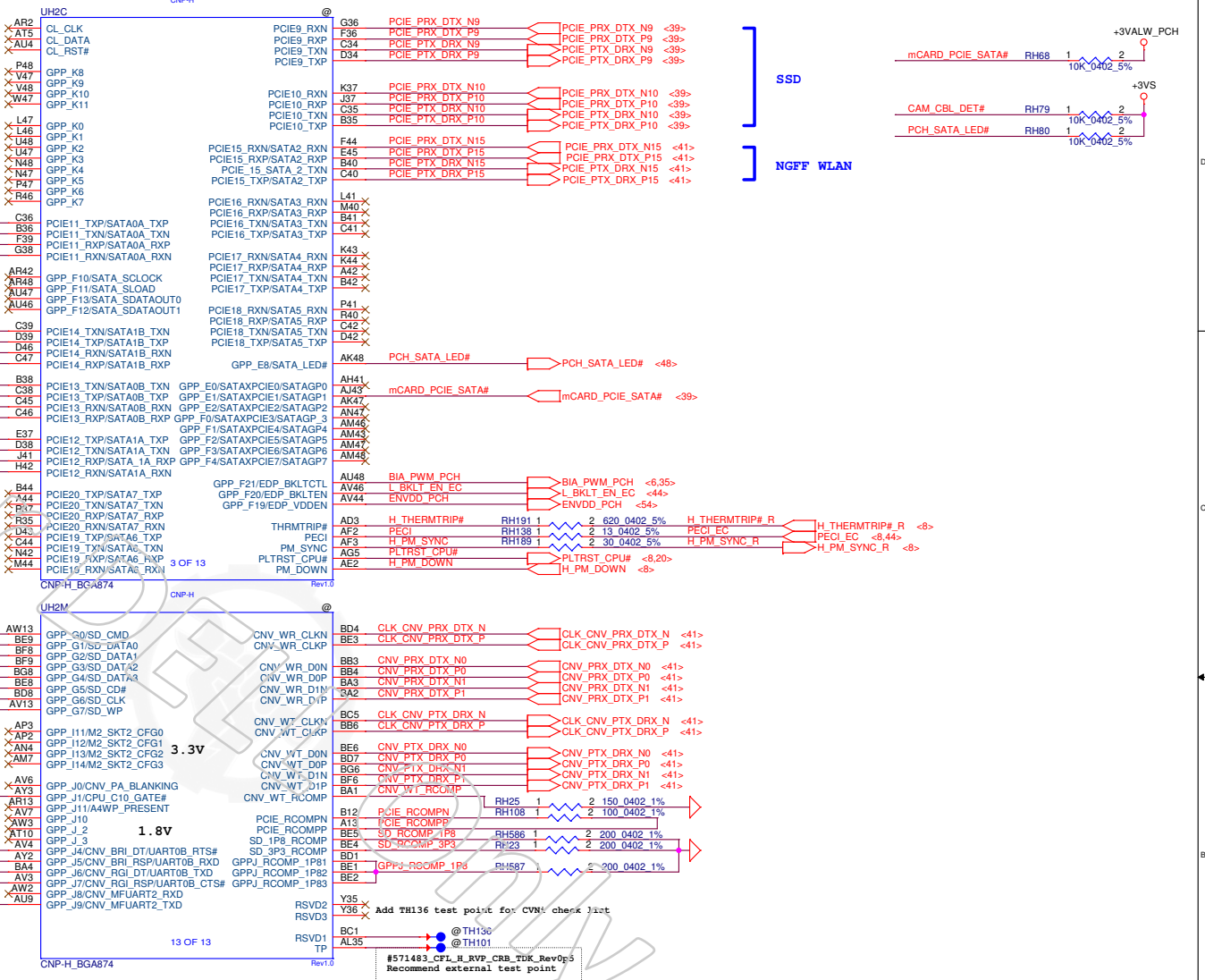
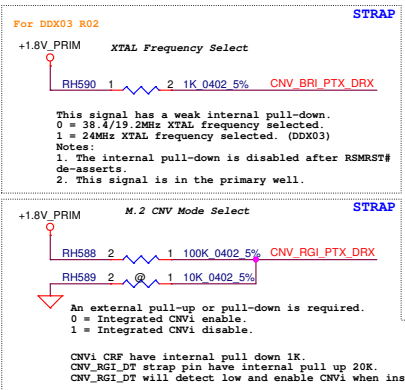
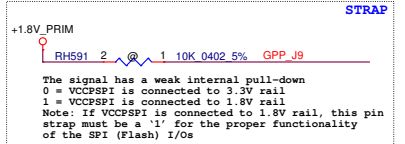
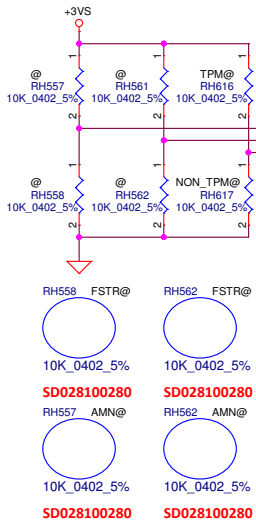
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TPM ID	TPM ID (GPP_G7)
SW TPM	0
HW TPM	1

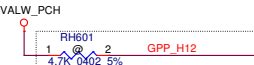
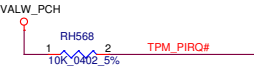
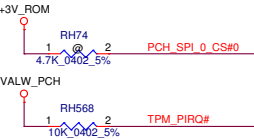
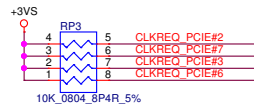
PROJECT ID	PROJECT ID1 (GPP_G3)	PROJECT ID2 (GPP_G4)
Firestar MLK	0	0
Firestar B	0	0
Armani MLK	1	0
Not Used	0	1



The 30 HSI0 lanes on PCH-H supports the following configurations:

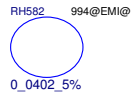
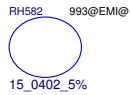
- Up to 24 PCIe* Lanes
 - A maximum of 16 PCIe* Ports (or devices) can be enabled
 - When a GBE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
 - Max PCIe* Ports (or devices) = 16 - GBE (0 or 1)
 - PCIe* Lanes 1-14 (PCIe* Controller #1), 15-24 (PCIe* Controller #2), 25-32 (PCIe* Controller #3), 33-42 (PCIe* Controller #4), 43-52 (PCIe* Controller #5), and 53-62 (PCIe* Controller #6) can be individually configured
- Up to 6 SATA Lanes
 - A maximum of 6 SATA Ports (or devices) can be enabled
 - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
 - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- Up to 10 USB 3.1 Lanes
 - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
- Up to 4 GbE Lanes
 - A maximum of 1 GbE Port (or device) can be enabled
- Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe* storage devices
 - x2 and x4 PCIe* NVMe SSD
 - x2 Intel® Optane™ Memory Device
 - See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers, configurations, and Lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support
- For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe* Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29			
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	SATA 0b	SATA 1a	SATA 1b	PCIe #15	PCIe #16	PCIe #17	PCIe #18	PCIe #19	PCIe #20	PCIe #21	PCIe #22	PCIe #23	PCIe #24
											GBE					GBE			GBE	GBE	GBE												
Intel® RST Support	No Support						No Support					Yes					No Support					Yes					Yes						

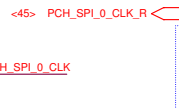


STRAP

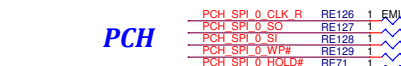
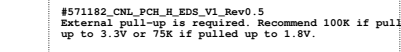
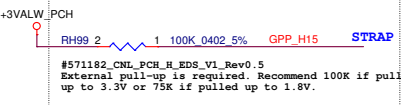
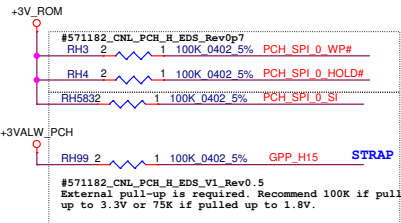
This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
1. This signal is in the primary well.
Warning: This strap must be configured to '0' if the eSPI or LPC strap is configured to '0'.



SD028150A80 SD028000080

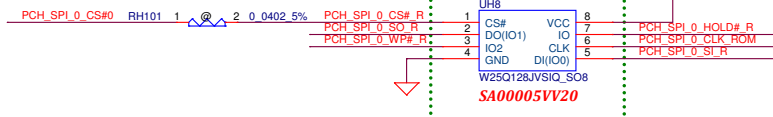


Reserve for RF



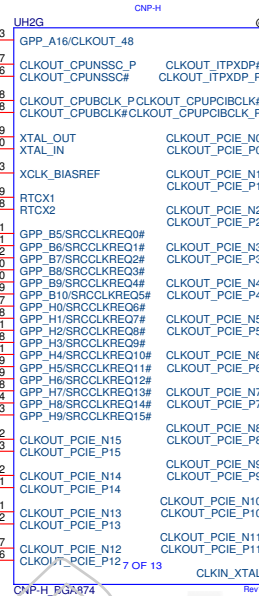
Close to UH8

SPI ROM FOR ME (16MByte)

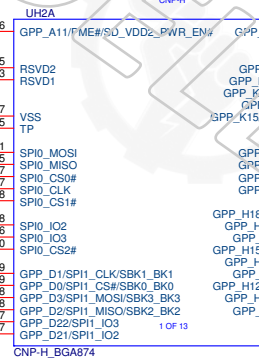


DVT2.
Change UH8 from SA00009R10 W25Q256JVEIQ_WSON8_8X6 to SA00005V20 W25Q128JVSQ_S08

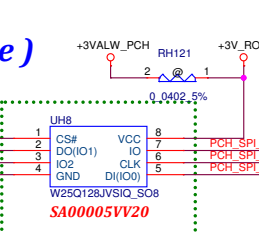
SPI ROM



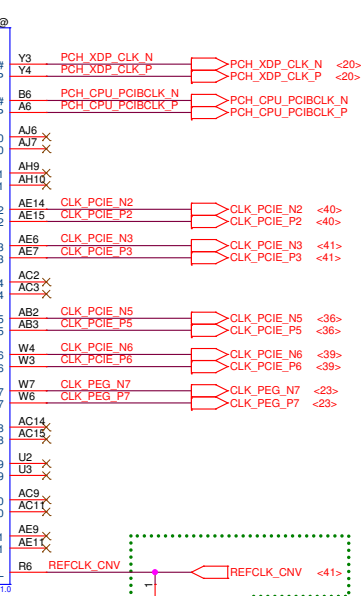
Rev1.0



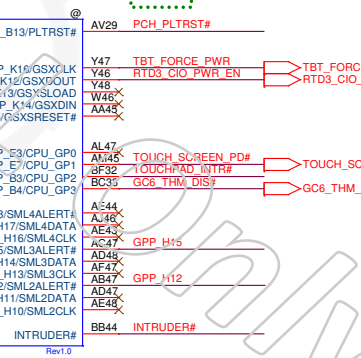
Rev1.0



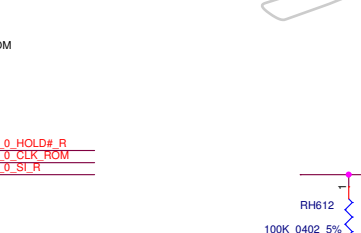
DVT2.
Change UH8 from SA00009R10 W25Q256JVEIQ_WSON8_8X6 to SA00005V20 W25Q128JVSQ_S08



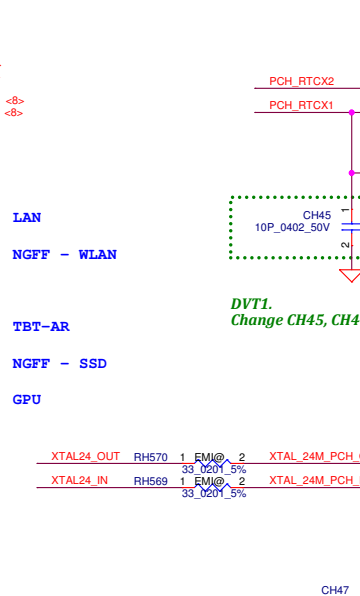
Rev1.0



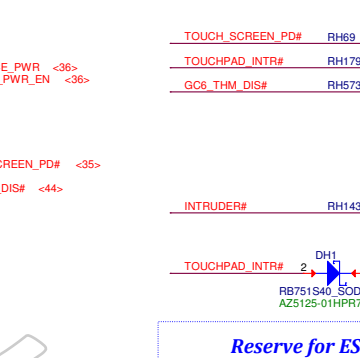
Rev1.0



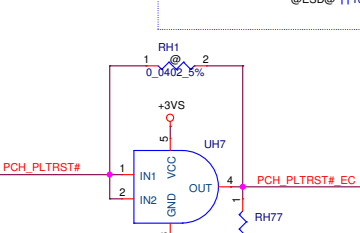
DVT2.
Change UH8 from SA00009R10 W25Q256JVEIQ_WSON8_8X6 to SA00005V20 W25Q128JVSQ_S08



Rev1.0

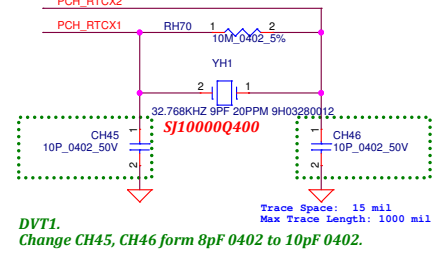


Rev1.0



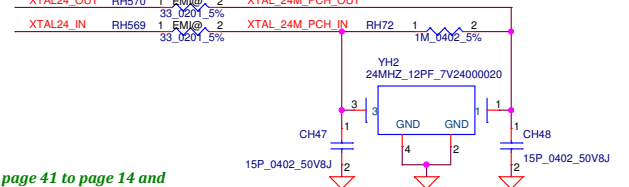
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RTC CRYSTAL

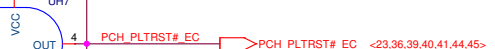
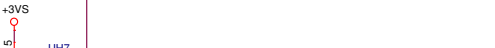
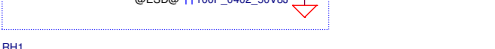
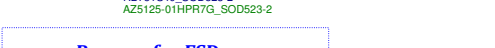
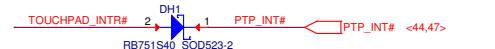
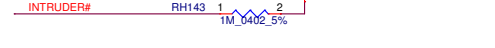
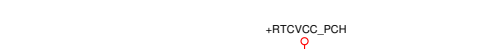
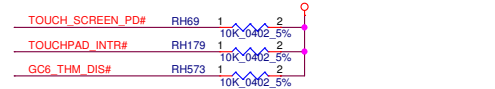


DVT1.
Change CH45, CH46 from 8pF 0402 to 10pF 0402.

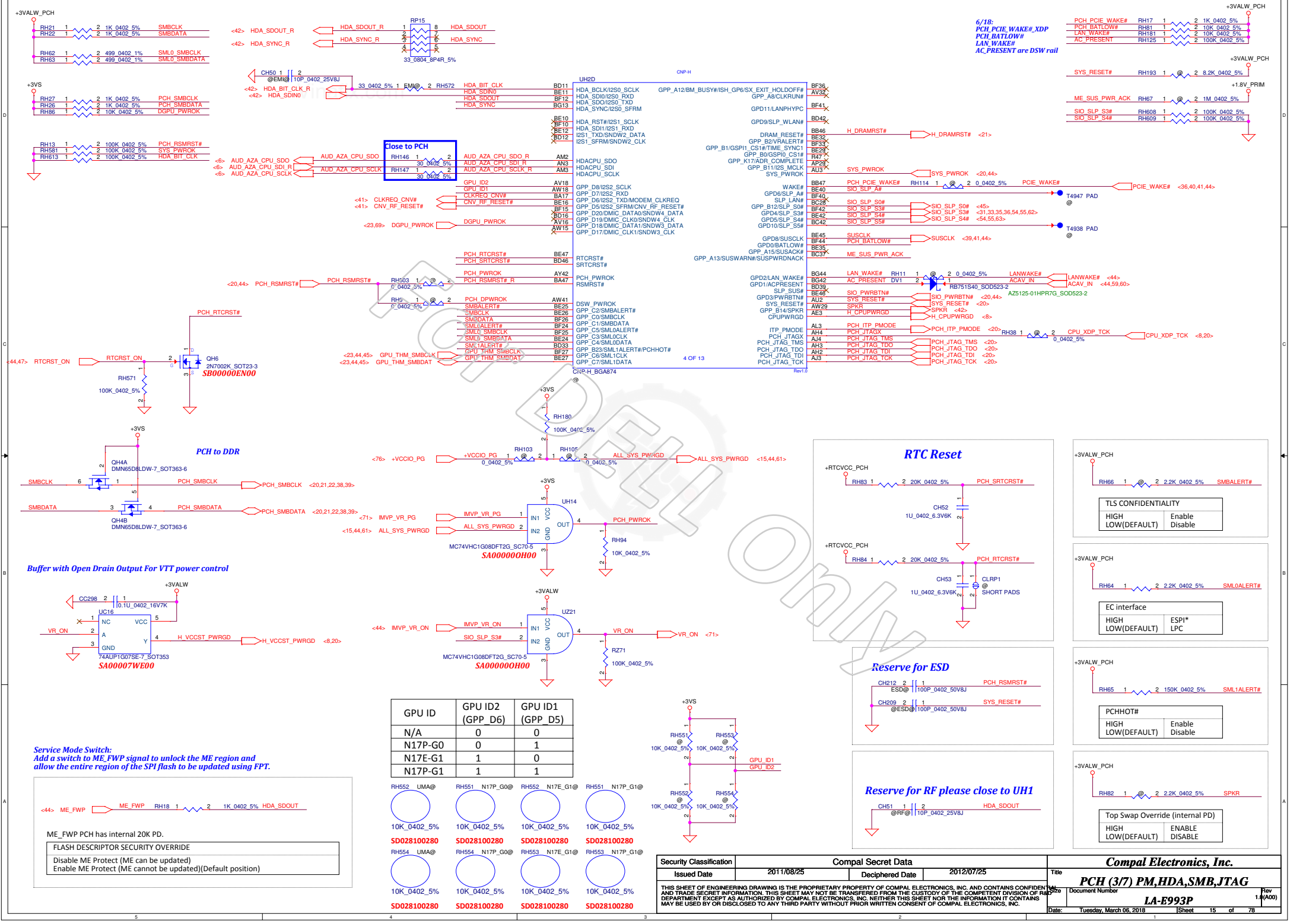
PCH CRYSTAL



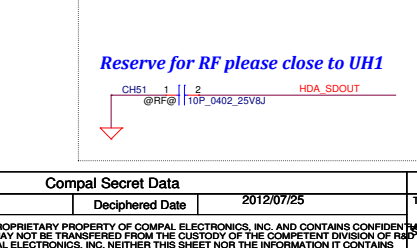
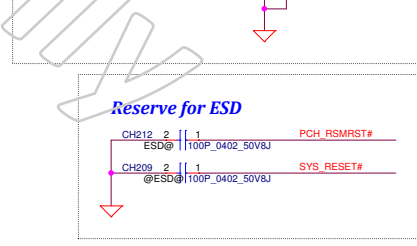
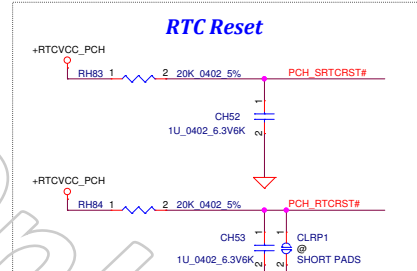
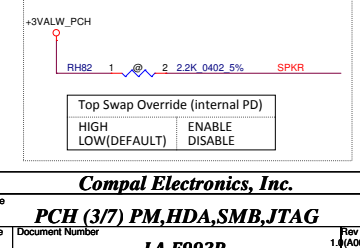
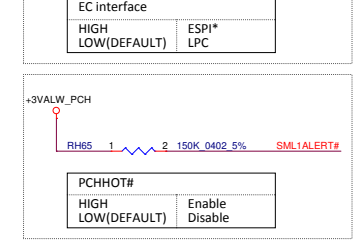
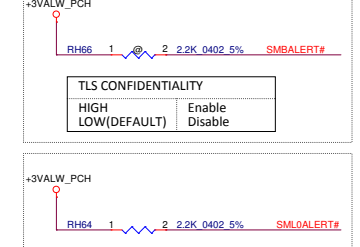
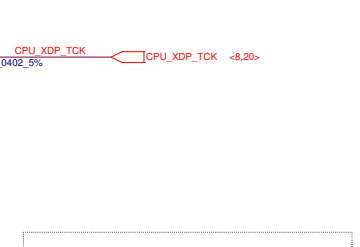
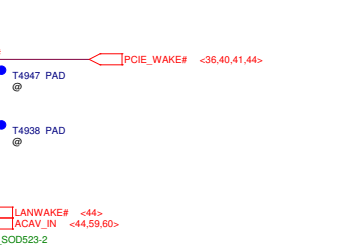
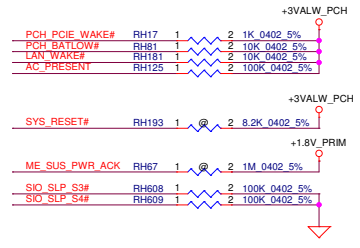
DVT1.
Move RN36 from page 41 to page 14 and connnet to net REFCLK_CNV.



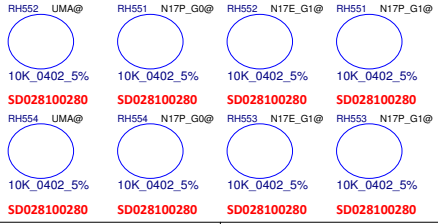
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	PCH (2/7) CLK,SPI,PLTRST	
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				LA-E993P	
				Date: Tuesday, March 06, 2018	Sheet 14 of 78



6/18:
PCH_PCIE_WAKE#_XDP
PCH_BATLOW#
LAN_WAKE#
AC_PRESENT are DSW rail



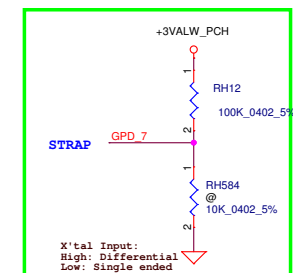
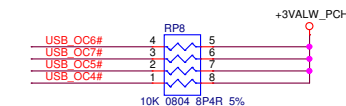
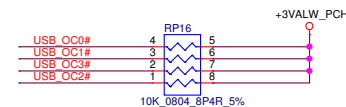
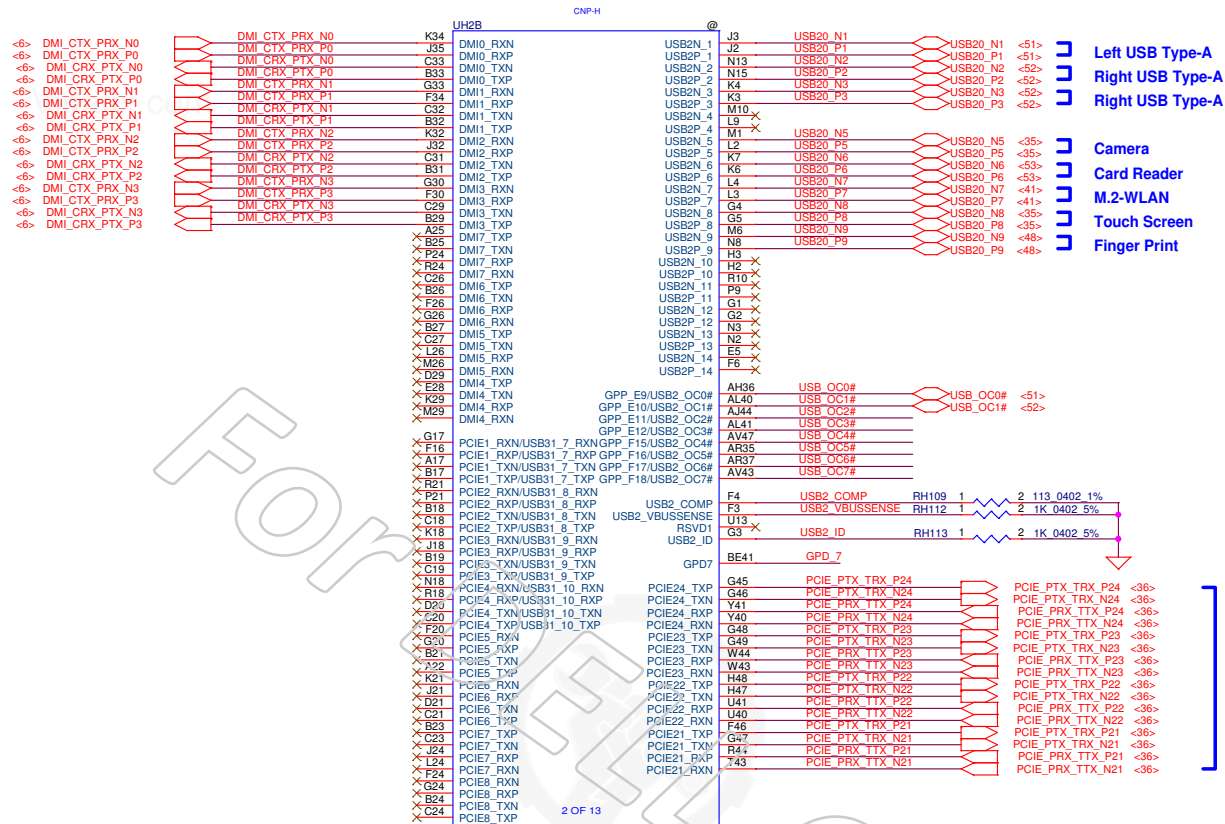
GPU ID	GPU ID2 (GPP D6)	GPU ID1 (GPP D5)
N/A	0	0
N17P-G0	0	1
N17E-G1	1	0
N17P-G1	1	1



Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
Disable ME Protect (ME can be updated)
Enable ME Protect (ME cannot be updated)(Default position)

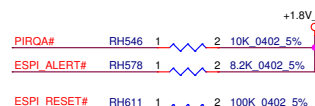
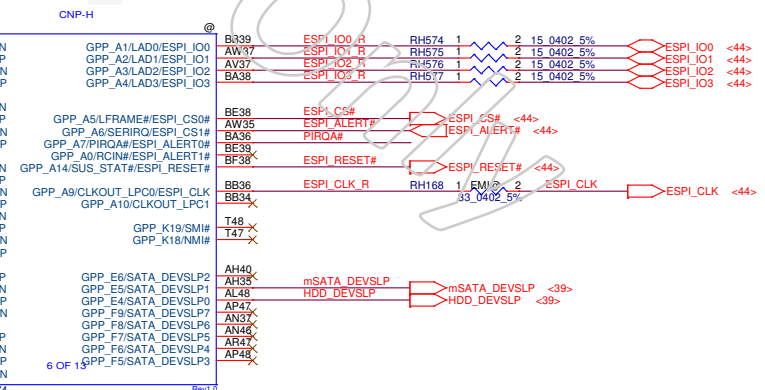


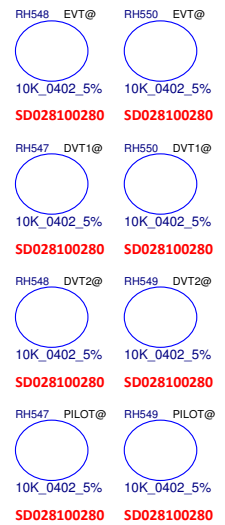
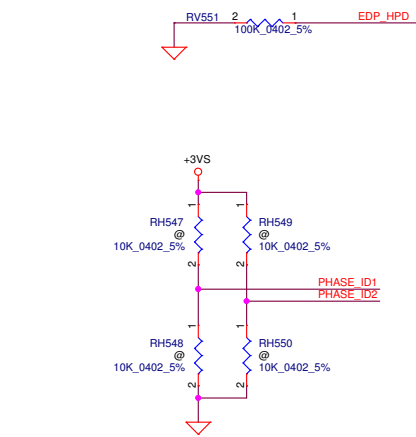
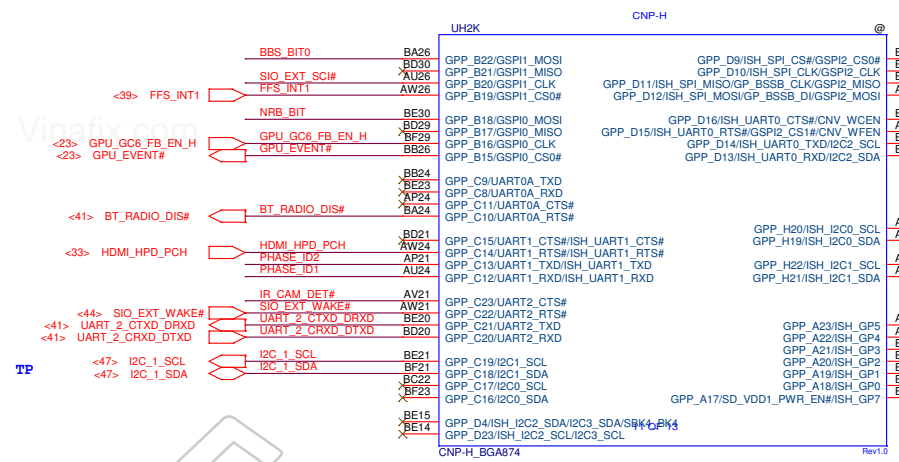
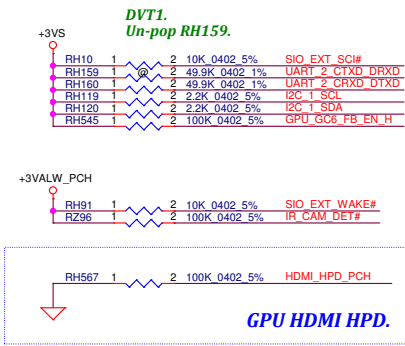
6/18: GPD_7 is DSW rail

Left USB Type-A

Right USB Type-A

Right USB Type-A



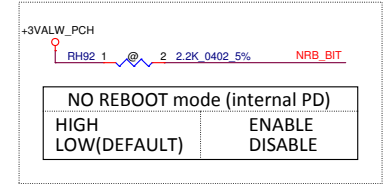
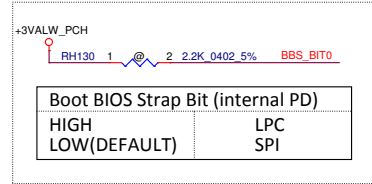


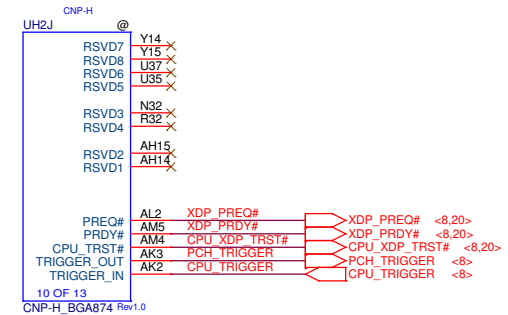
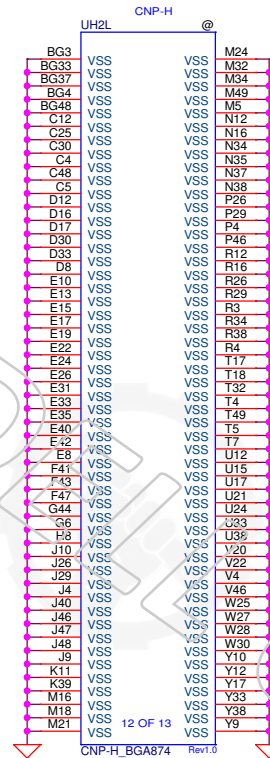
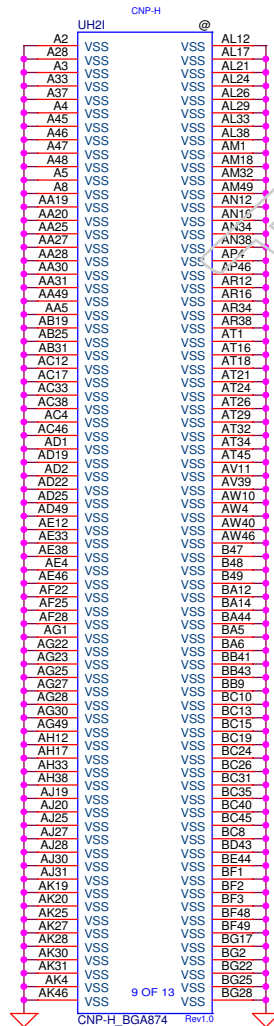
PHASE ID	PHASE ID2 (GPP_C13)	PHASE ID1 (GPP_C12)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot	1	1



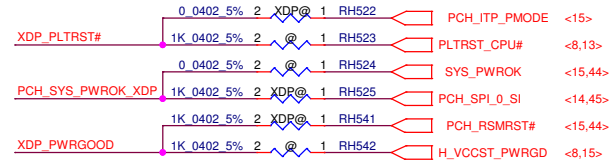
Table 5-11. DD1 Disabling and Termination Guidelines

Port	Strap	How to Enable PortΩ	How to Disable PortΩ
Port 1	DDPB_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 3	DDPD_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect





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						Size		Document Number		Rev	
								LA-E993P		1.0(400)	
						Date:		Tuesday, March 06, 2018		Sheet 19 of 78	

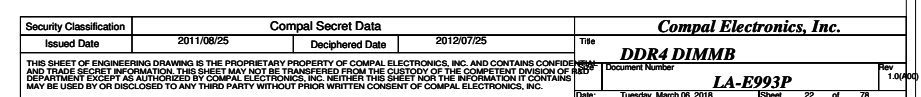


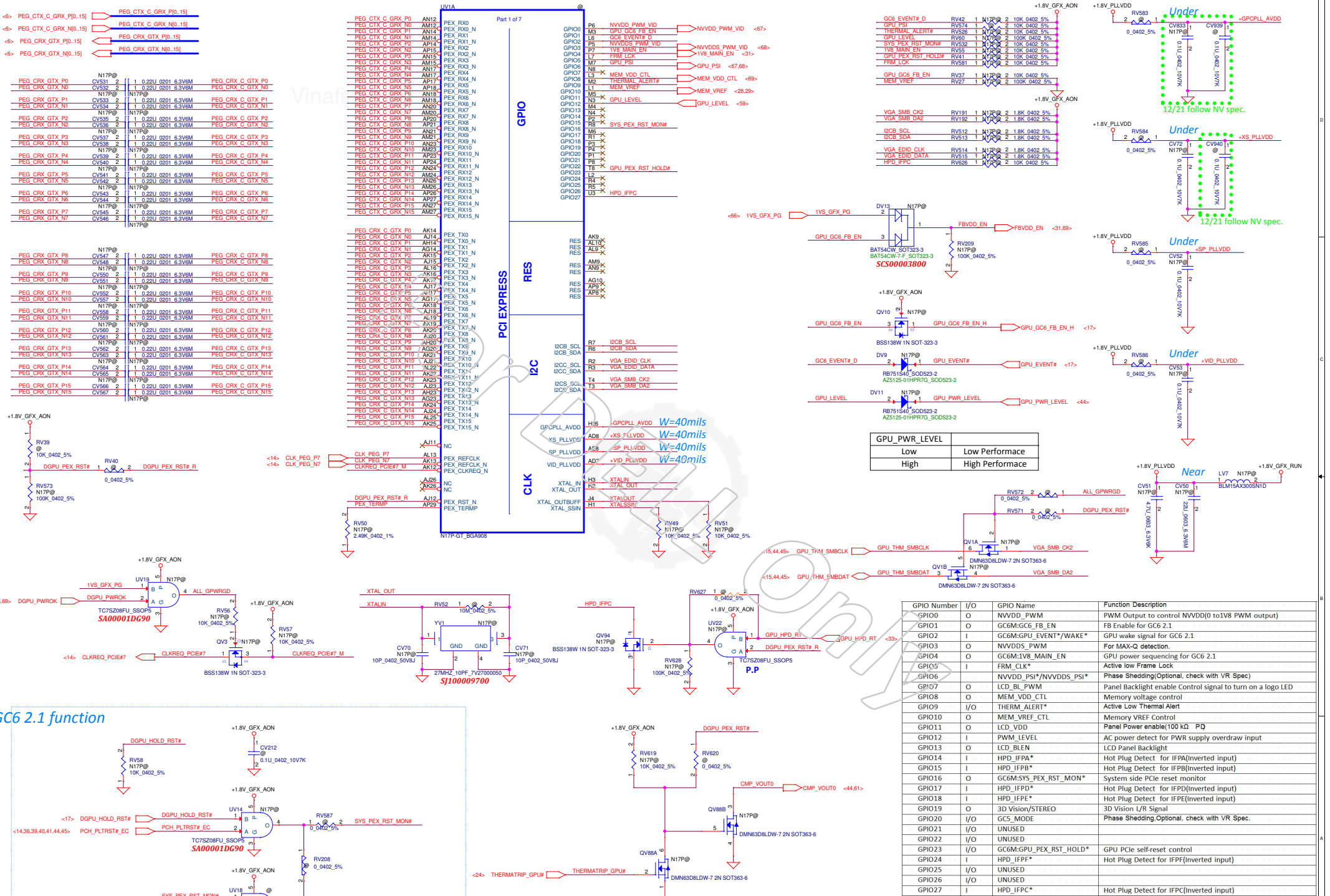
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<15,21,22,38,39> PCH_SMBC1_K
<15> PCH_JTAG_TCK
<8,15> CPU_XDP_TCK
```



40	ITPCLK/HOOK4	CLKOUT_ITPXPDP_P	I	Coffee Lake
42	ITPCLK#/HOOK5	CLKOUT_ITPXPDP_N	I	Coffee Lake
44	VCC_OBS_AB	PCH V1.0A	NA	
46	HOOK6/RESET#	ITP_PMODE	I	Coffee Lake
48	HOOK7/DBR#	SYS_RESET#	O	Coffee Lake
50	GND	GND	NA	

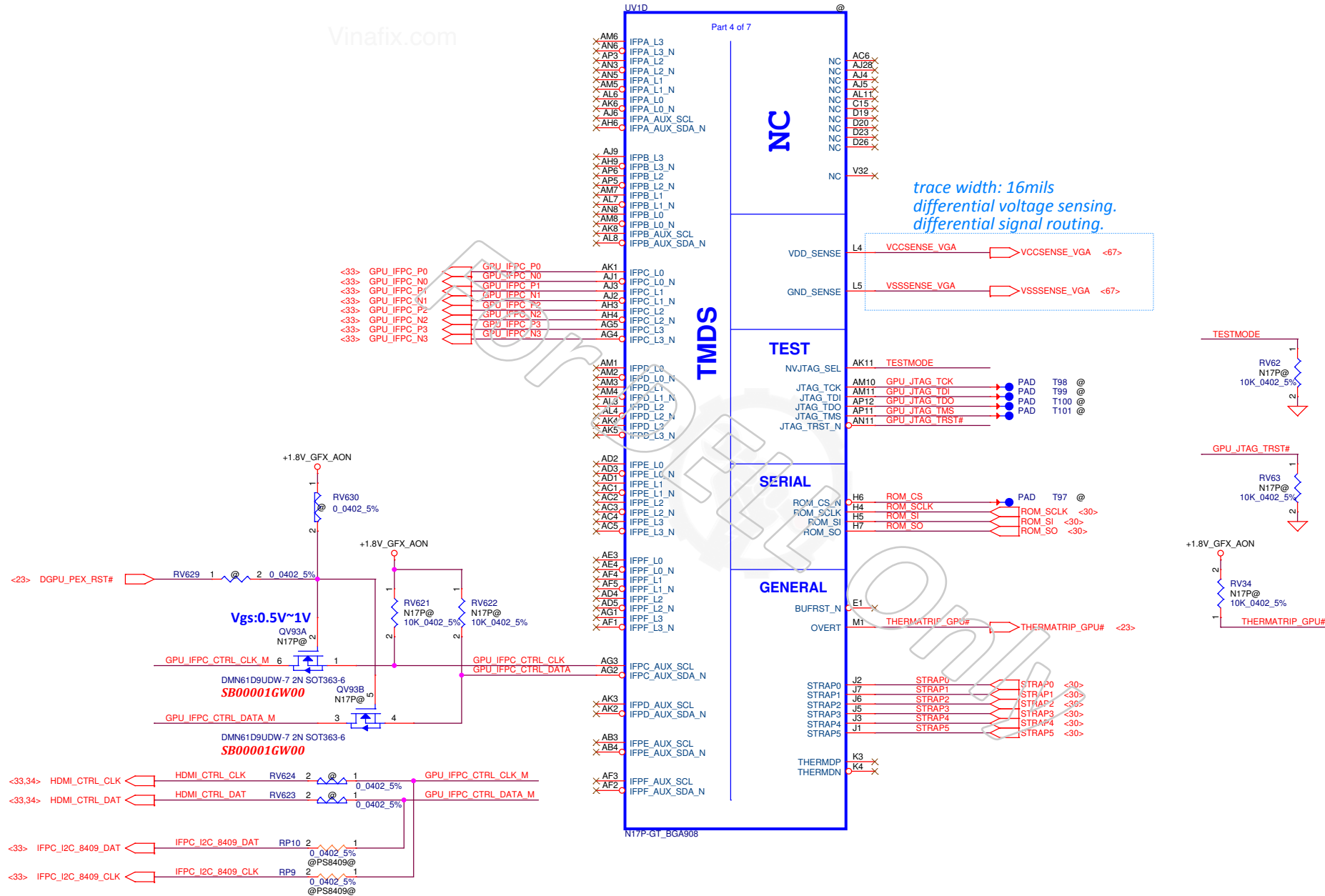
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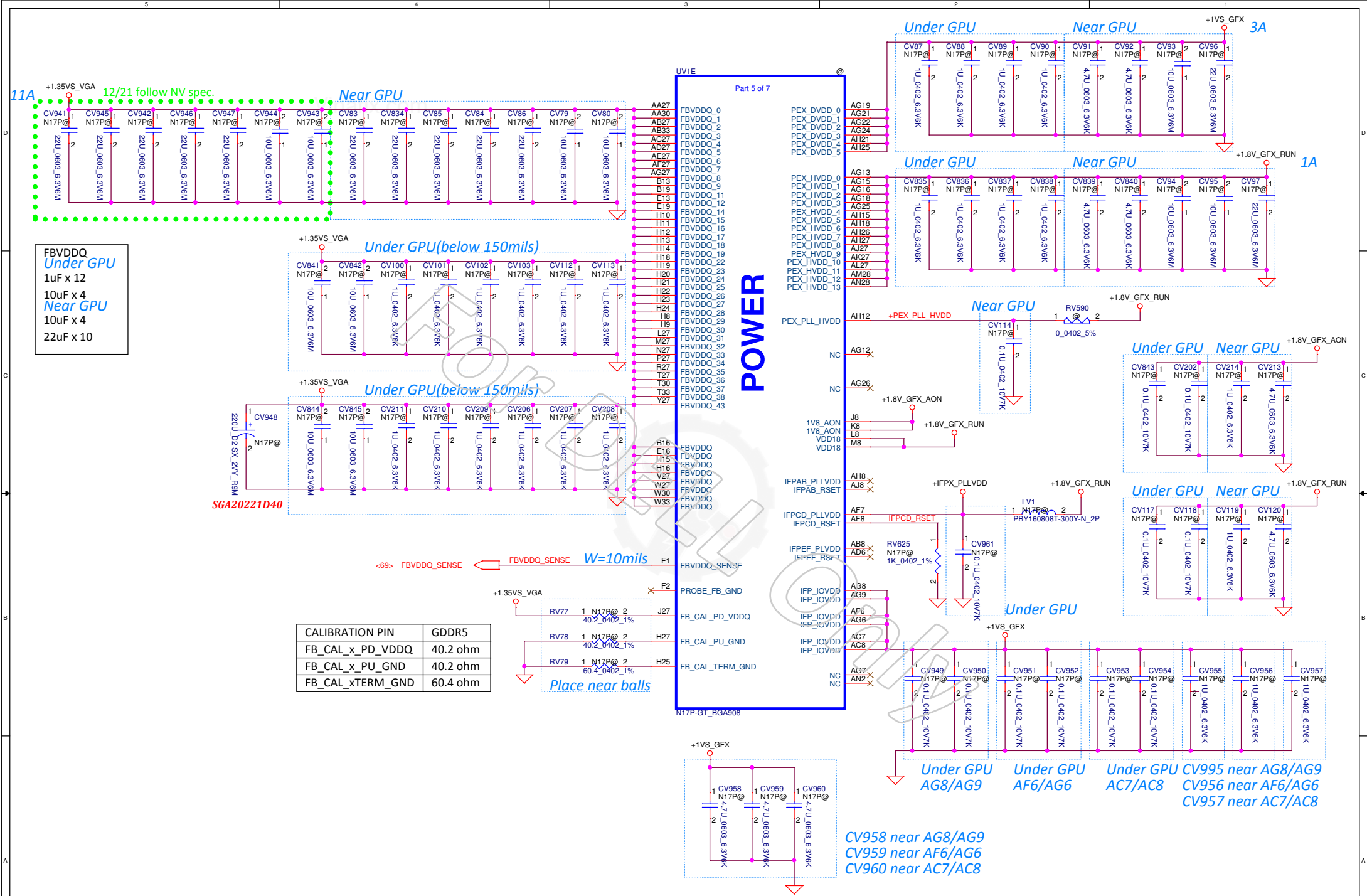


GC6 2.1 function

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Issued Date		2017/01/06								Compal Electronics, Inc.	
										N17P PCIe/DAC/GPIO	
										LA-E993P	
										Size	
										Doc Number	
										Rev	
										1.4(40)	
										Date	
										Tuesday, March 06, 2018	
										Sheet	
										23	
										of	
										8	



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date:	Tuesday, March 06, 2018
				Sheet	24 of 78

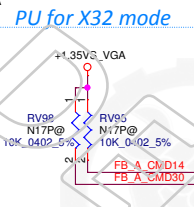
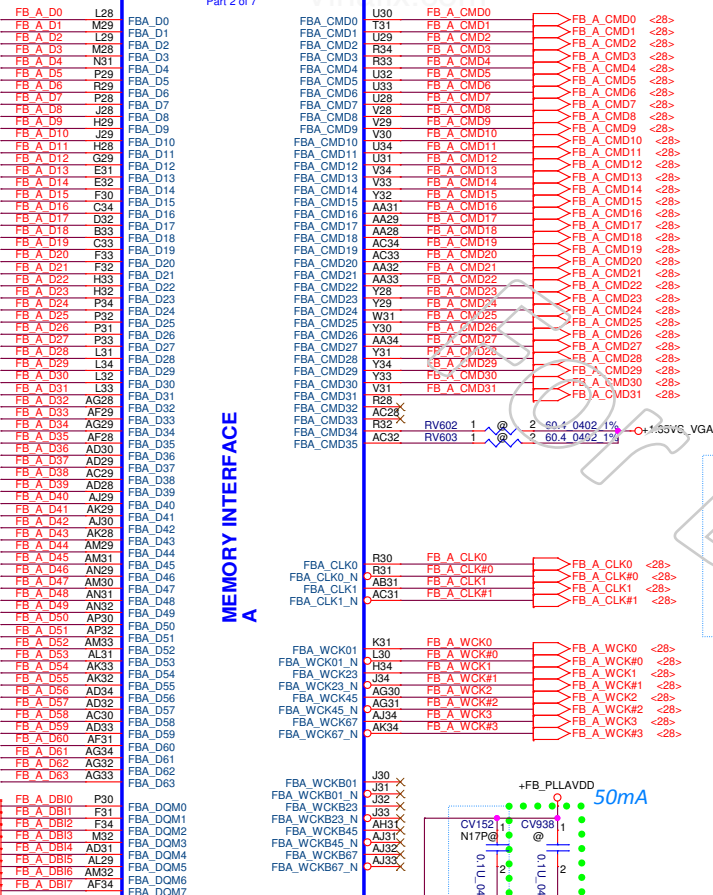


<28> FB_A_D[0..63] FB_A_D[0..63]
<28> FB_A_EDC[7..0]

<29> FB_B_D[0..63] FB_B_D[0..63]
<29> FB_B_EDC[7..0]

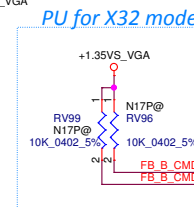
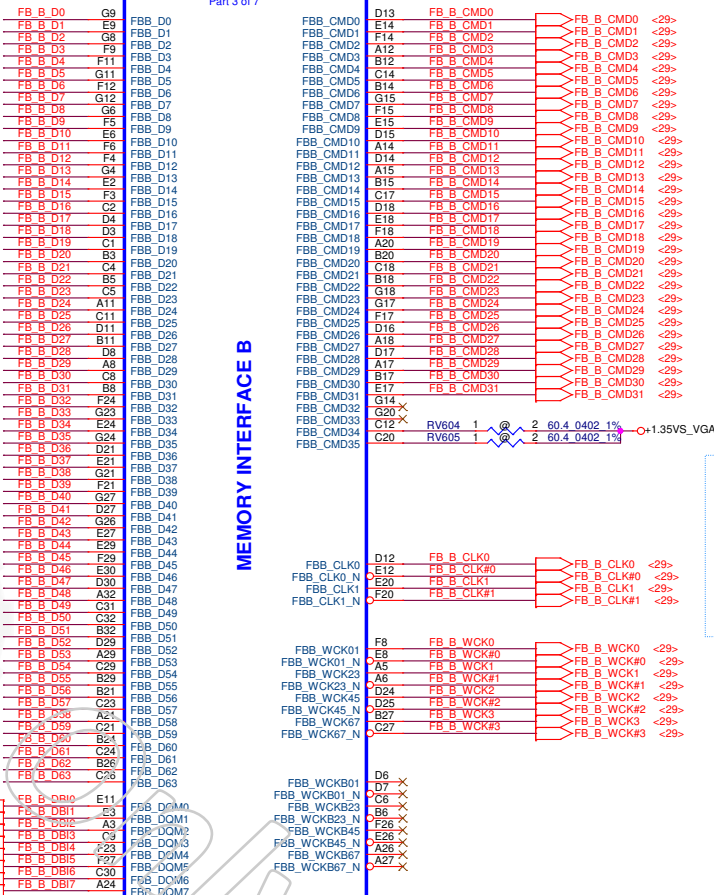
UV1B

Part 2 of 7



UV1C

Part 3 of 7



FB_REFPLL_AVDD

FB_A_PLL_AVDD

FB_VREF

FB_REFPLL_AVDD

FB_A_PLL_AVDD

FB_VREF

FB_REFPLL_AVDD

FB_A_PLL_AVDD

FB_VREF

FB_REFPLL_AVDD

FB_B_PLL_AVDD

FB_VREF

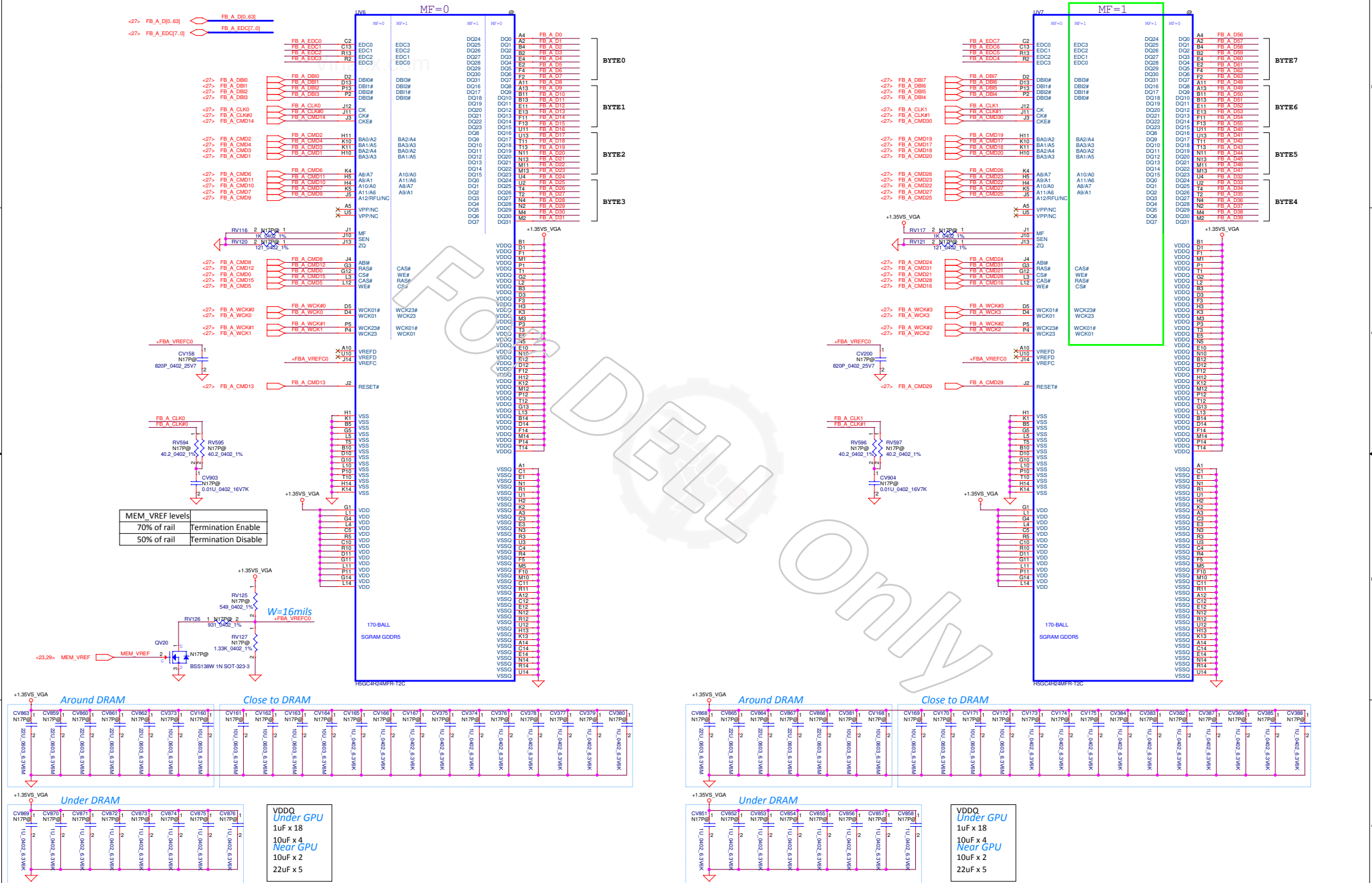
FB_REFPLL_AVDD

FB_B_PLL_AVDD

FB_VREF

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Date:	Tuesday, March 06, 2018	Sheet	27	of 78

Memory Partition A - Lower 32 bits



Memory Partition A - Lower 32 bits

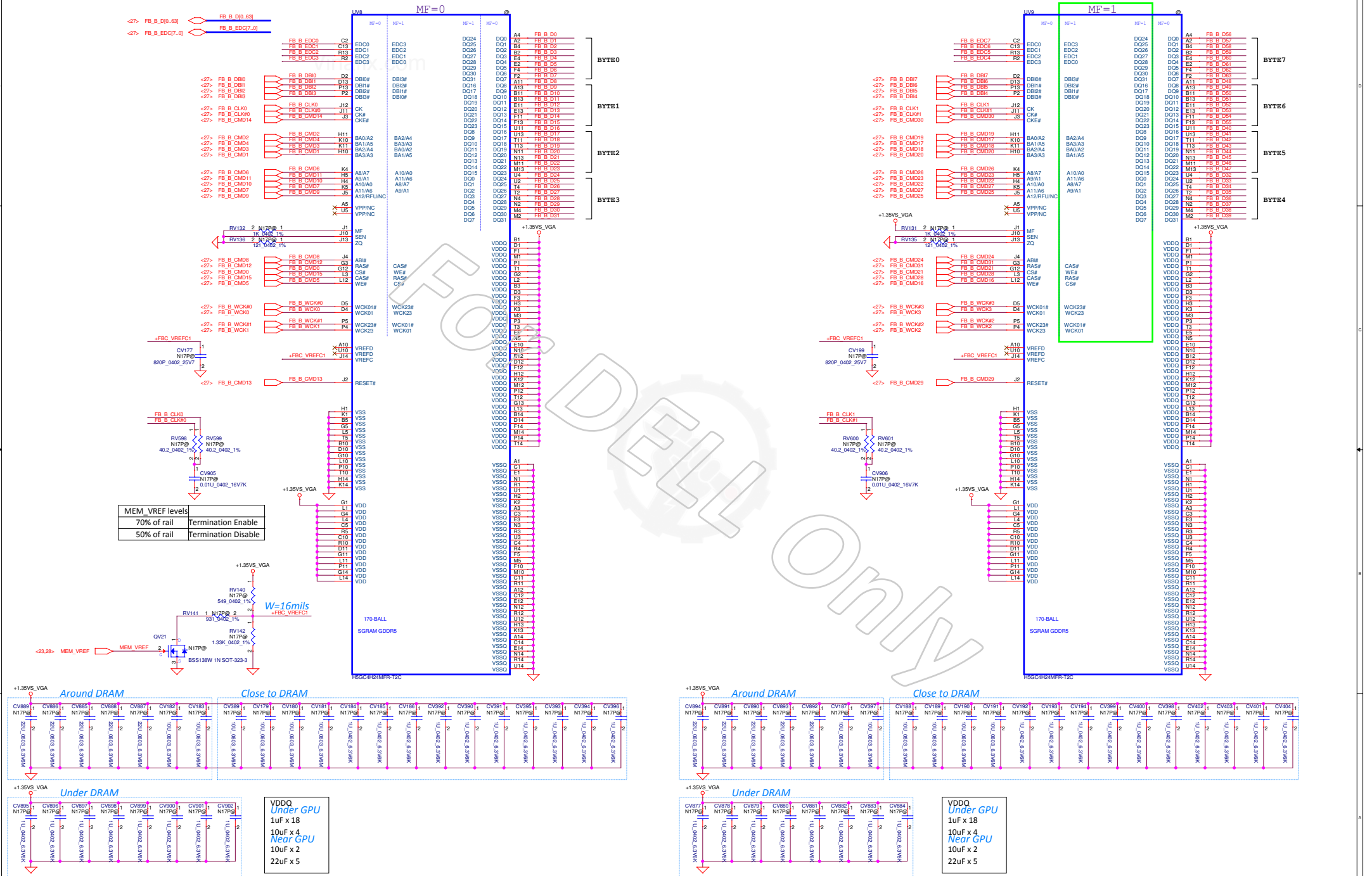


Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revisior	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V ²	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
4 Gb	128Mx32	1.35V and 1.5V ²	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production ready
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production ready
			Micron	EDW4032BAG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production ready

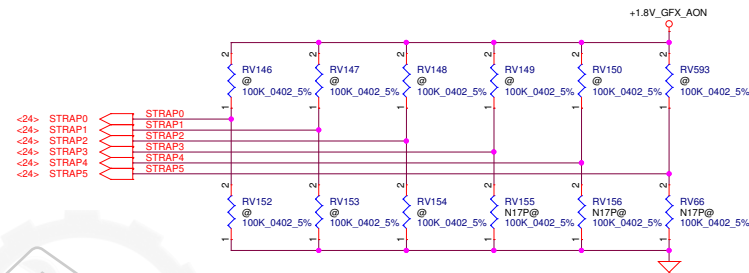


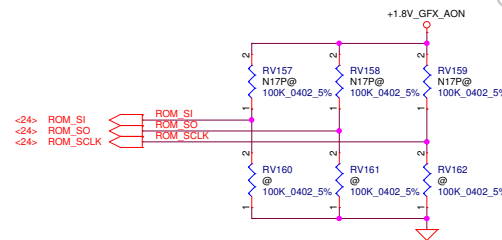
Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (i.e. DMI, DP or DVI)			See This Row of Table 5.5
Total Enabled for Audio (HDMI, DP or DVI)			
		Is IFPD used? (Only supports eDP.)	
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0

No other configurations are supported.

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
All other Strap Configurations				(Reserved)			

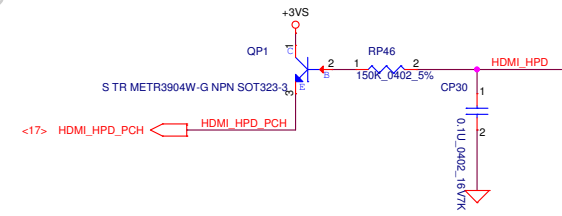
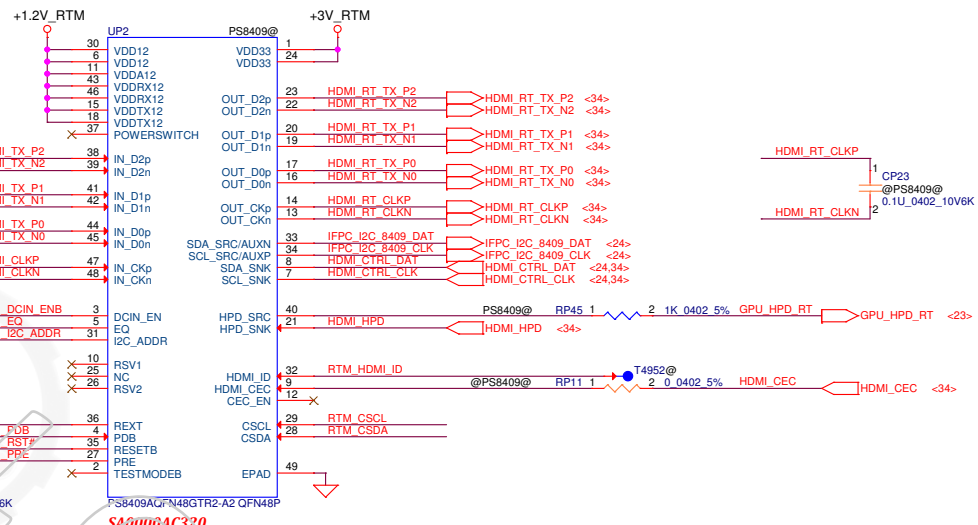
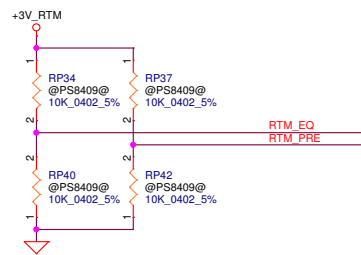
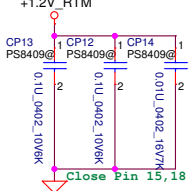
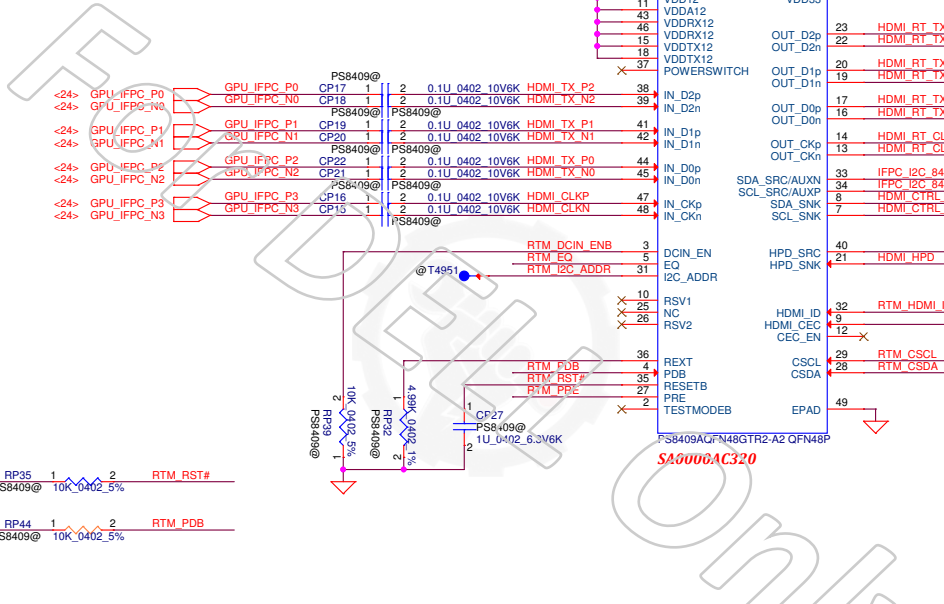
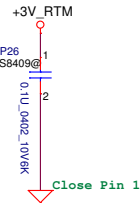
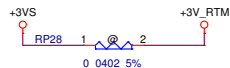


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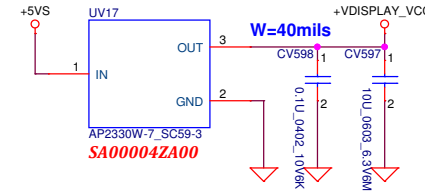
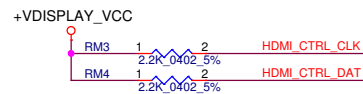
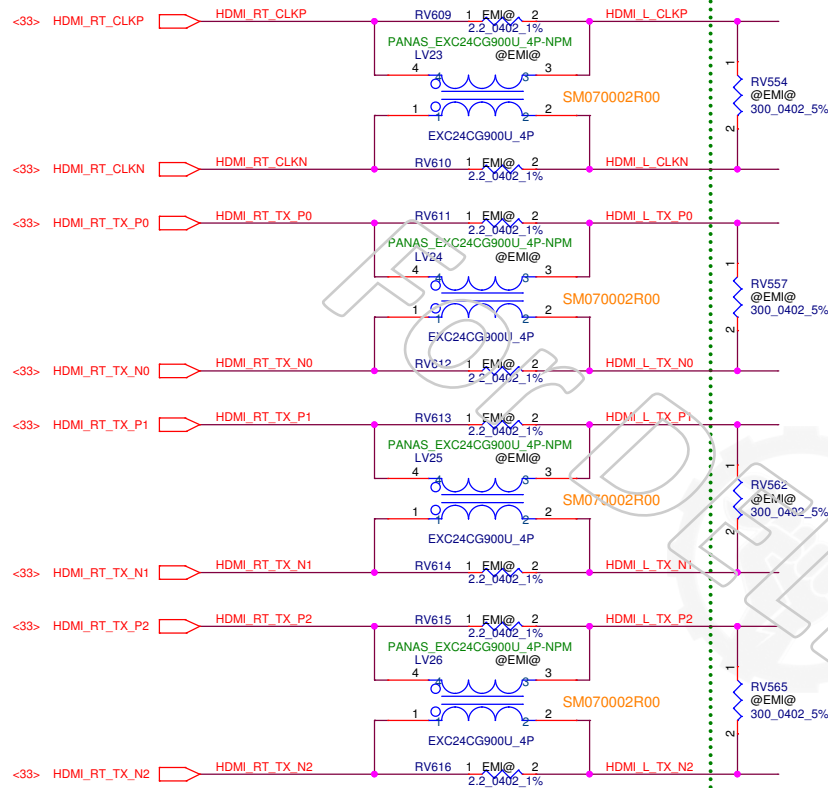
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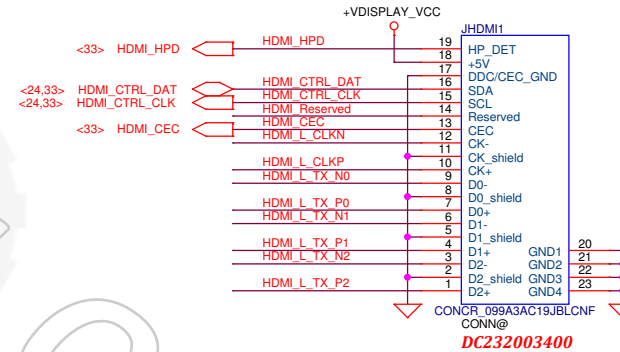
Vinafix.com

Place close to JHDMI1

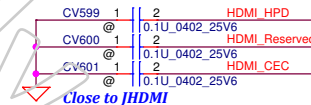
DVT1.
Move RV554, RV557, RV562, RV565
close to HDMI connector.



HDMI conn

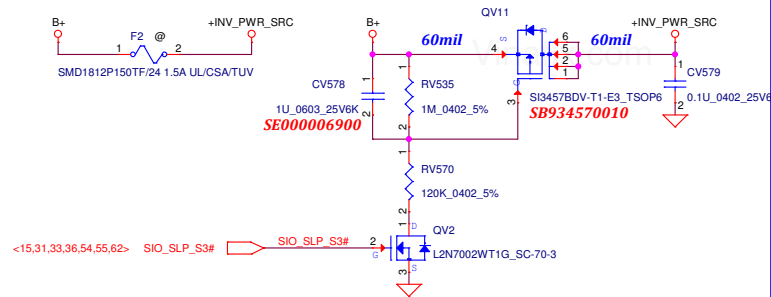


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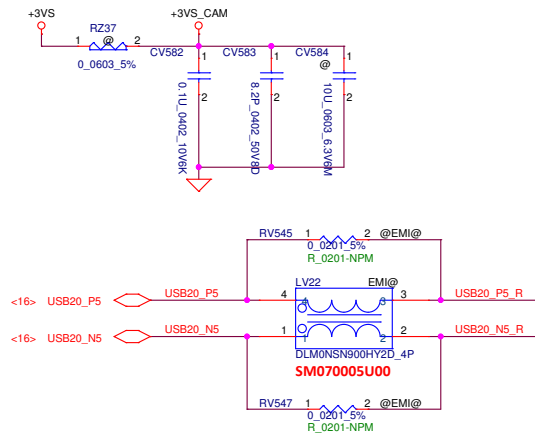


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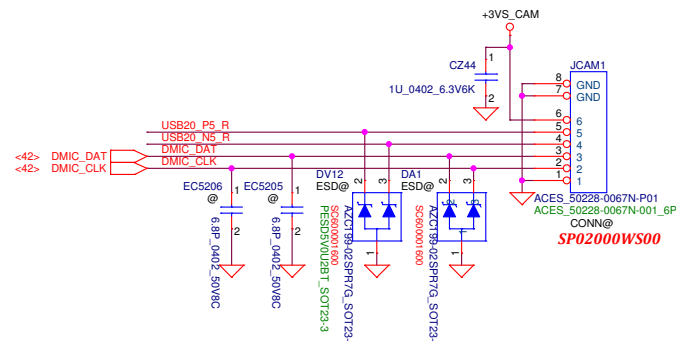
LCD backlight PWR CTRL



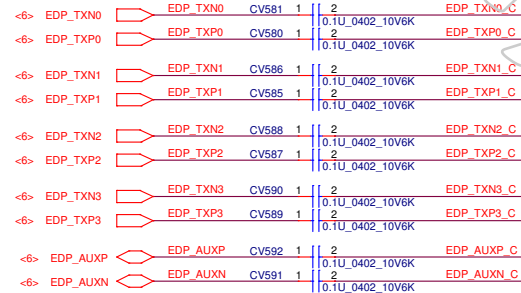
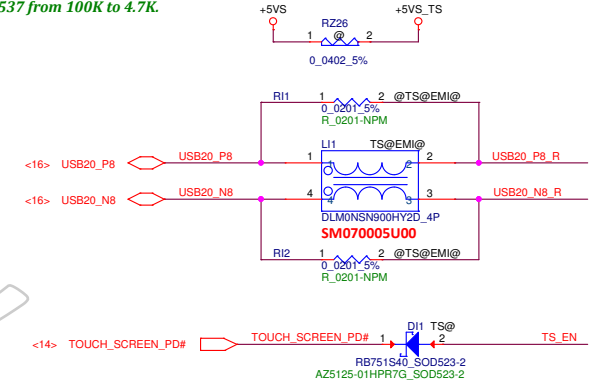
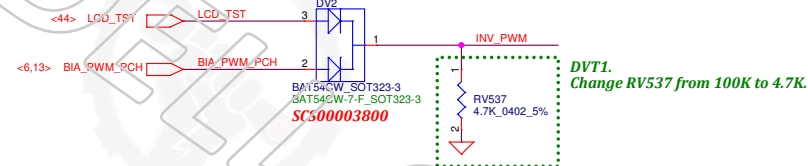
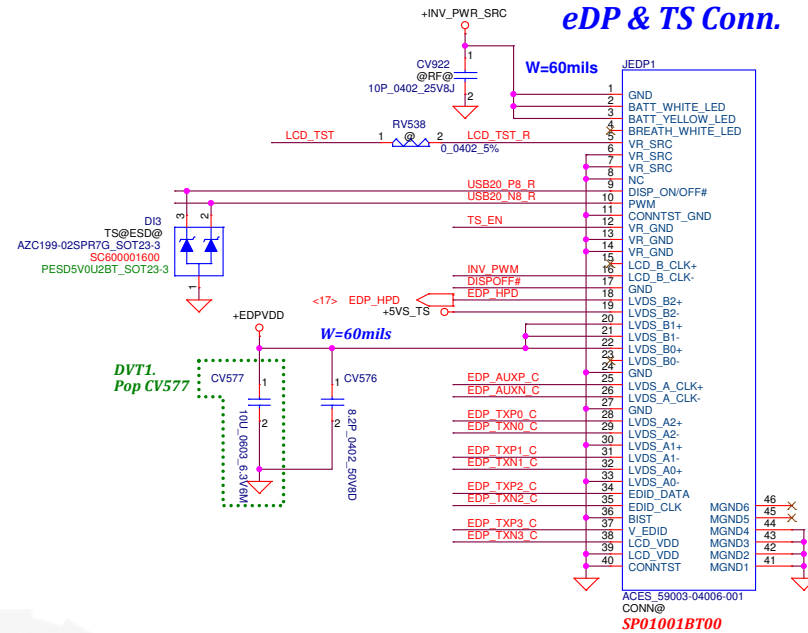
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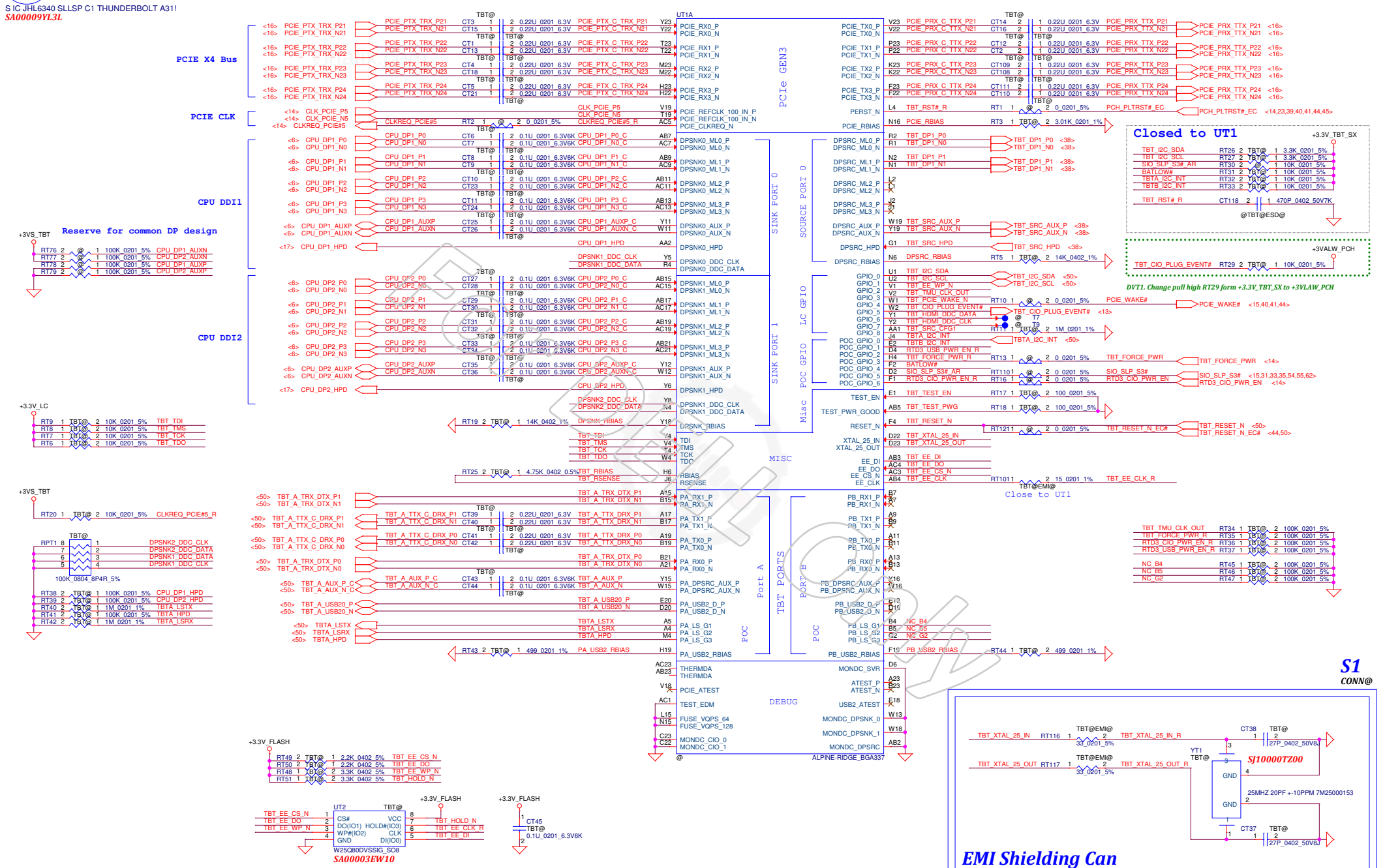
CCD +DMIC Connector



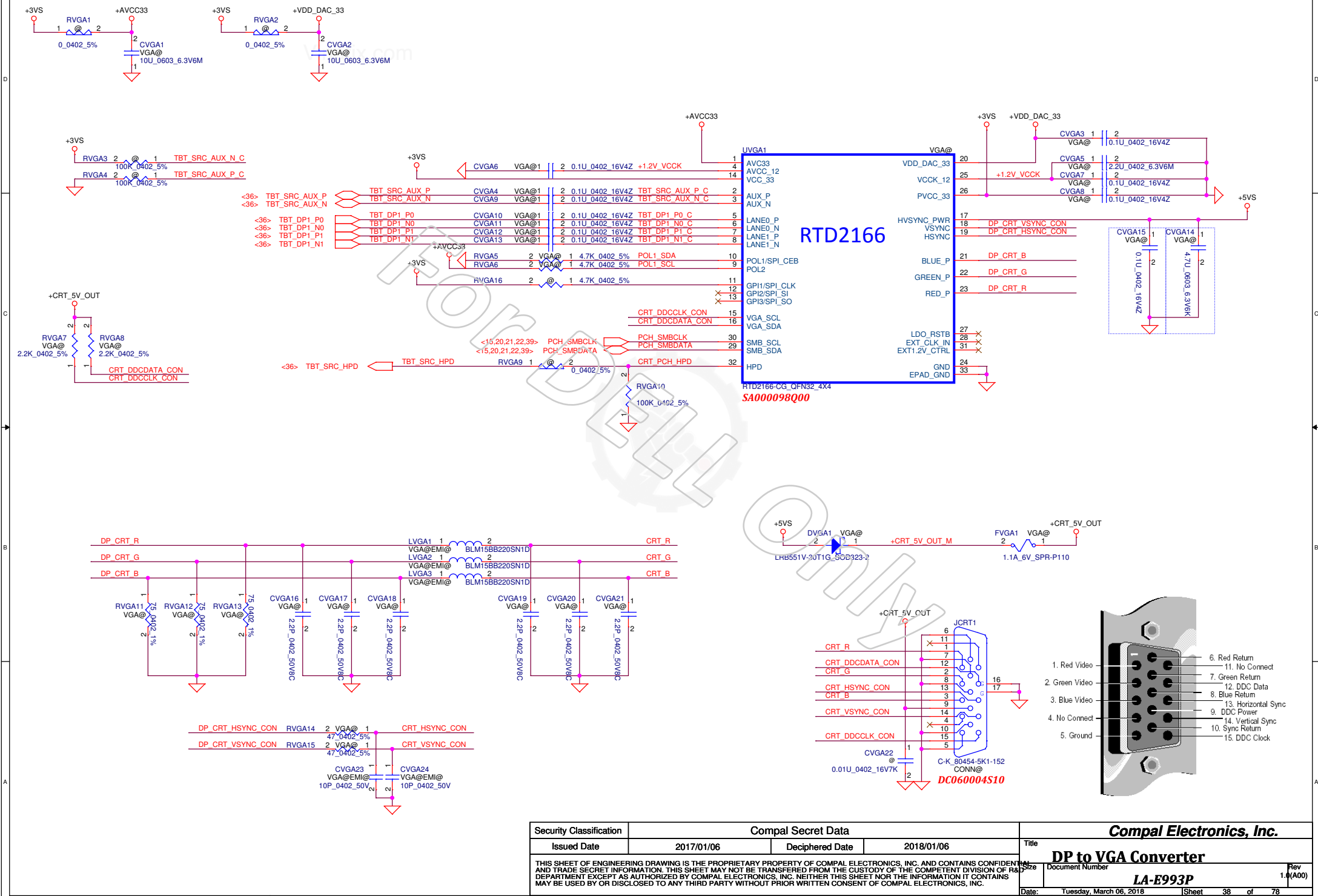
eDP & TS Conn.



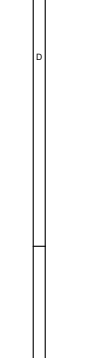
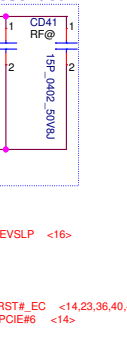
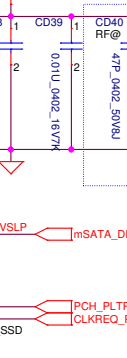
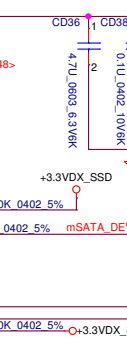
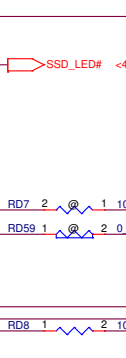
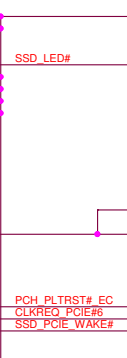
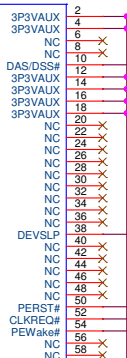
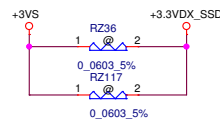
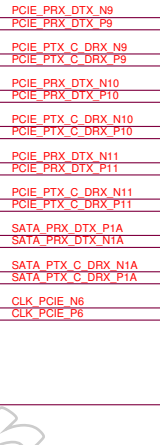
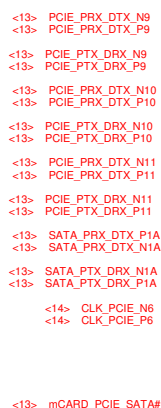
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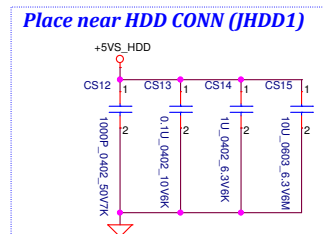
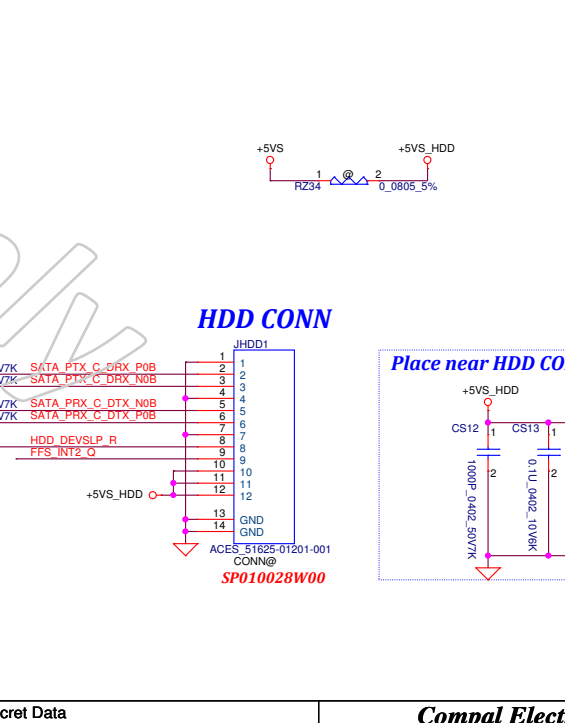
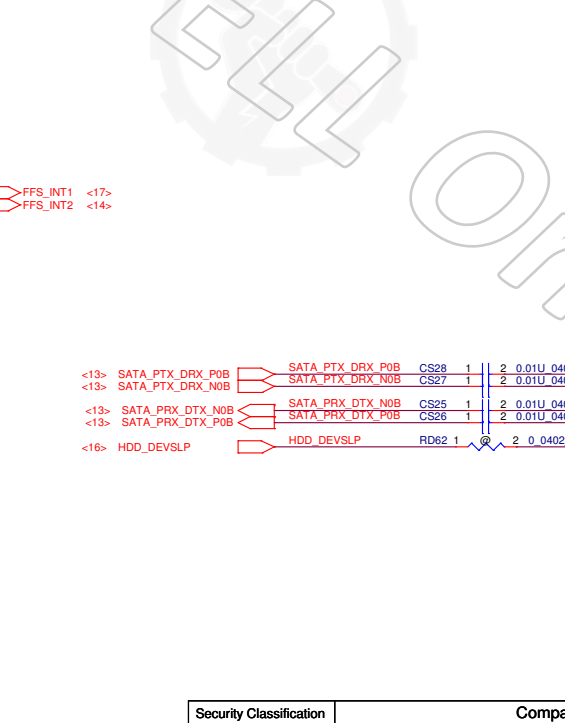
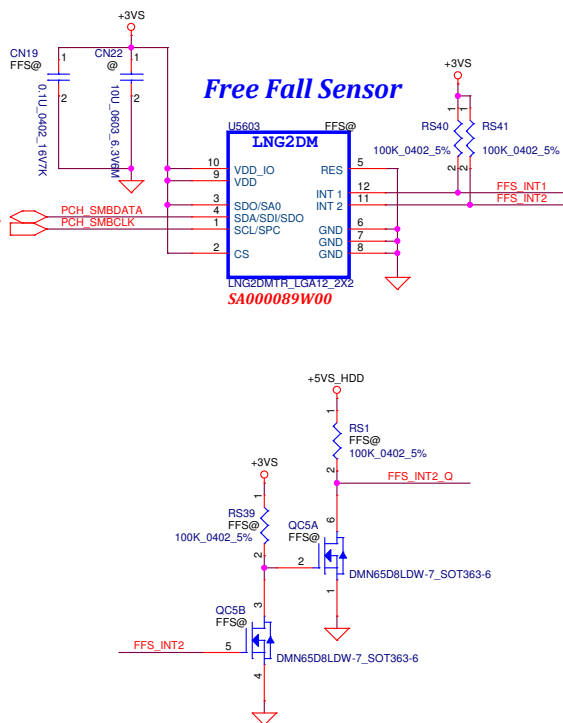
Main Func = DP to VGA Converter



A

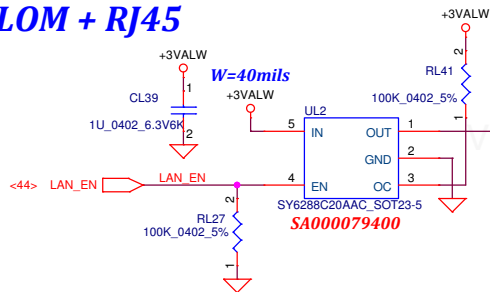


Name	Type	Description
DEVSLP₀ GPP_E4	OD	<p>Serial ATA Port (0) Device Sleep: This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to PCH's internal pull-up resistor to the SATA device per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.</p> <p>Design Constraint: As per PDG, no external Pull-up or Pull-down termination required when used as DEVSLP.</p> <p>Note: This pin can be mapped to SATA Port 0.</p>

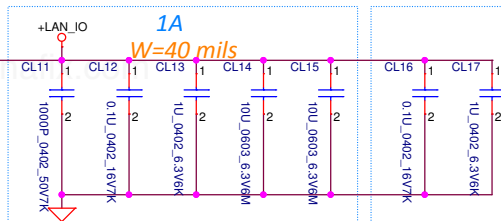


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LOM + RJ45

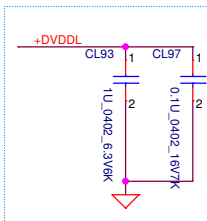


+LAN_IO rising time : >1ms and <100ms

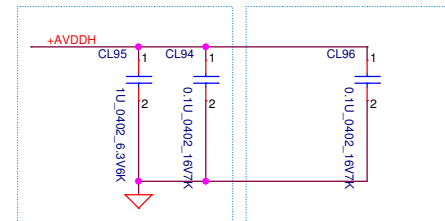


close to UL1 pin1

close to UL1 pin16

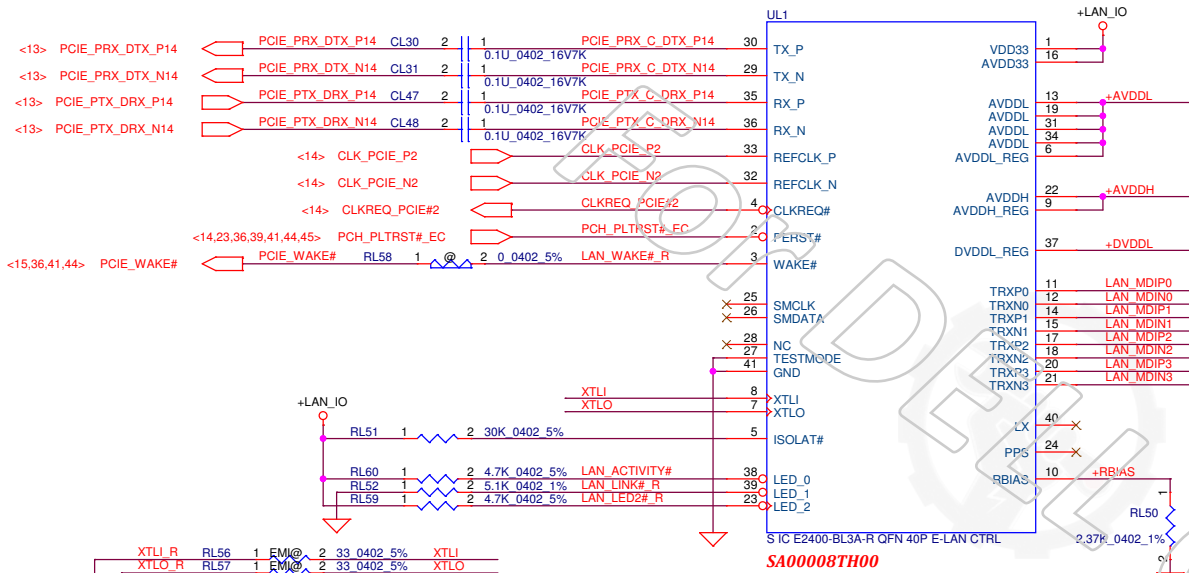


close to UL1 pin37

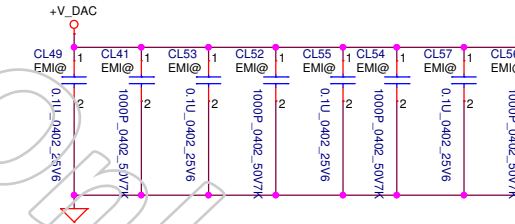
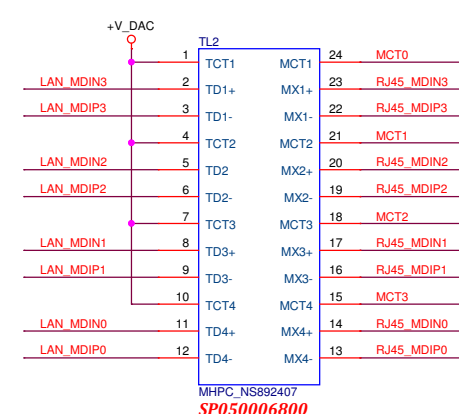


close to UL1 pin9

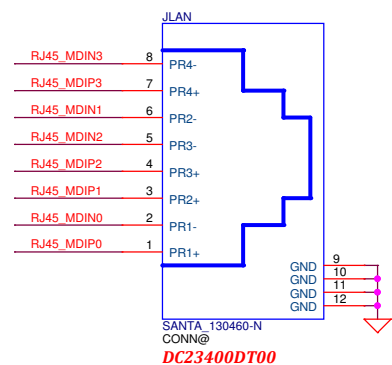
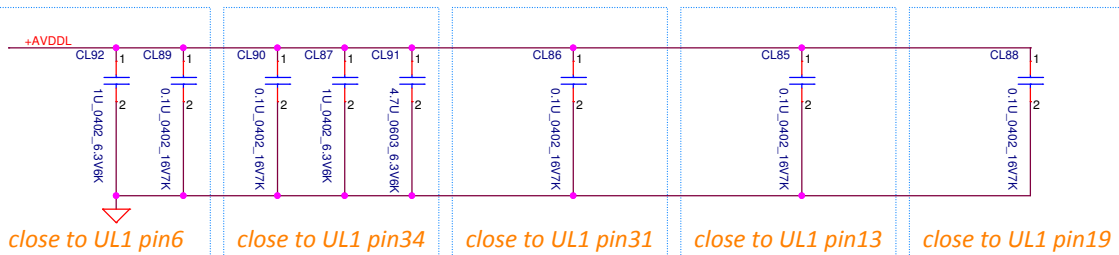
close to UL1 pin22



Killer E2500 SA0000A6L00

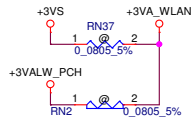


Place close to MCT pin



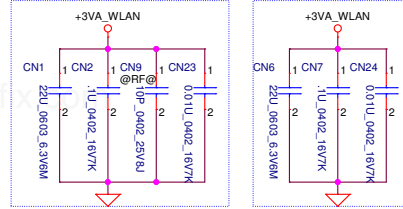
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M.2 Key-E (WLAN + BT)



6/18:
+3VALW_PCH is the same with +3VALW_DSW

Close to JNGFF1.2&4 Close to JNGFF1.64&66



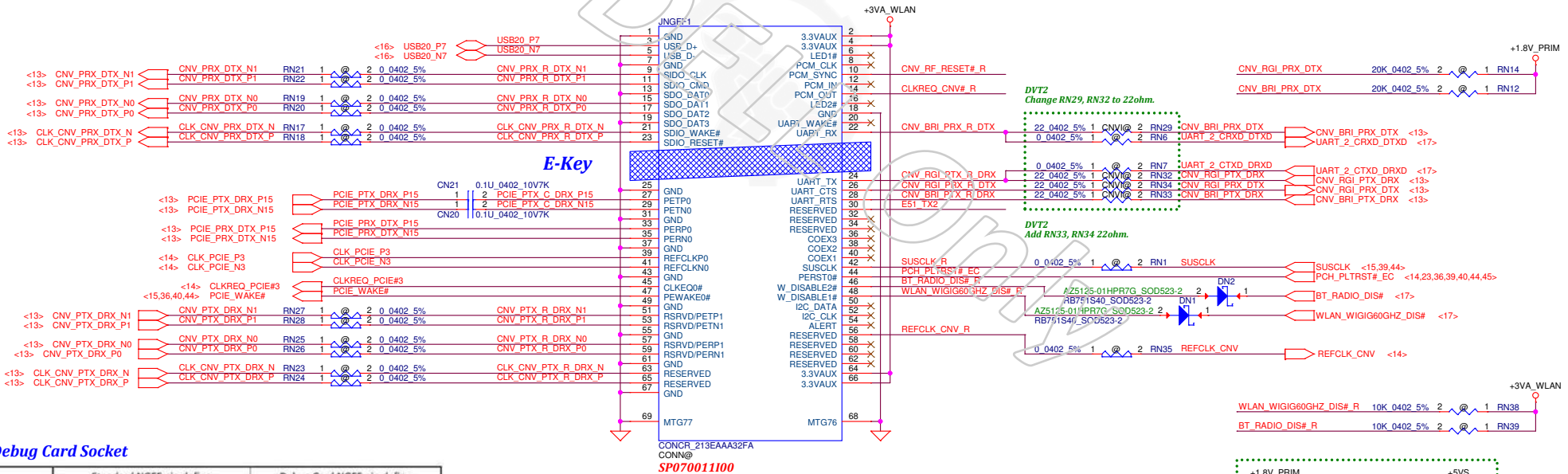
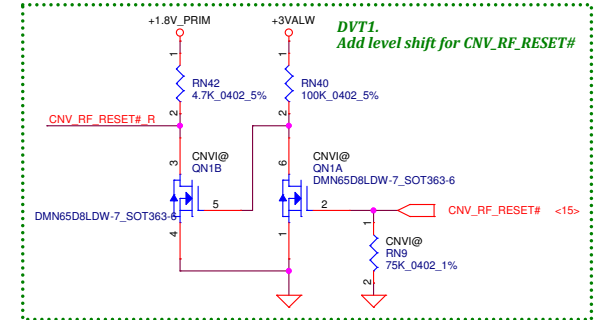
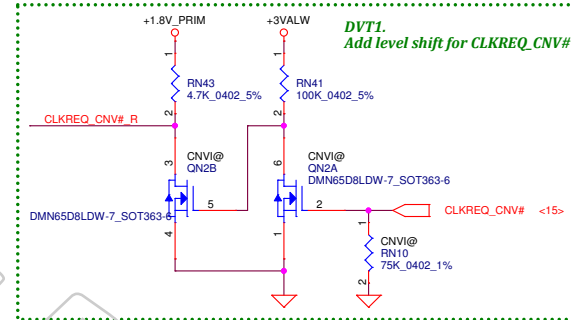
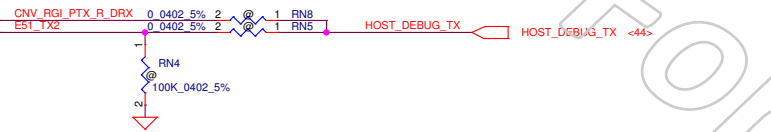
9.1.10 Connectivity module power control

The connectivity module power supply pins shall be connected directly to the rail DSW.

To ensure proper operation of the integrated connectivity module, the use of a power switch to control the M.2 module power shall be avoided. The Jefferson Peak module is not compatible with the SLP_WLAN control signal. Note that the Jefferson Peak module was designed with low-leakage power, and therefore does not require any external power control to be used during normal operation.

Debug Crad Port80:
If need to use Debug card to check port80 code, please pop RN8 and un-pop RN32!!!

Reserve for NGFF Debug Card

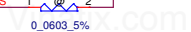


Key-E Debug Card Socket

	Standard NGFF pin define	Debug Card NGFF pin define
3.3VAUX	2, 4, 72, 74	2, 4, 56, 58
GND	1, 7, 18, 33, 39, 45, 51, 57, 63, 69, 75	1, 7, 10, 17, 23, 29, 35, 41, 47, 53, 59
NGFF_UART_TX	22	14
NGFF_UART_RX	32	16
EC_TX_P80DATA	38	22
EC_RX_P80CLK	40	24
PLT_RST#	52	36
NGFF_I2C_DATA	58	42
NGFF_I2C_CLK	60	44

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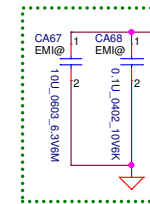
A



Speaker trace width >40mil @ 2W4ohm speaker power



Reserve for RF
Close pin3



[Close pin41](#) [Close pin](#)

Place close to Pin 26



Layout Note: Width>40mil, to improve Headphome Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.



```
moat
```

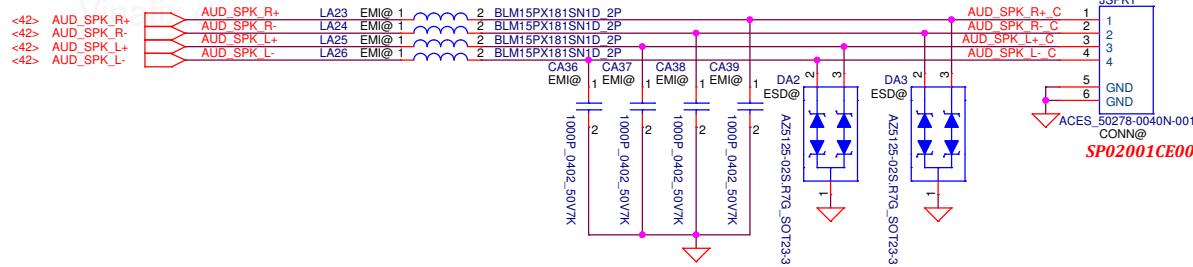


FINAL SIZE R&D	Document Number LA-E993P	Rev 1.0 (A00)
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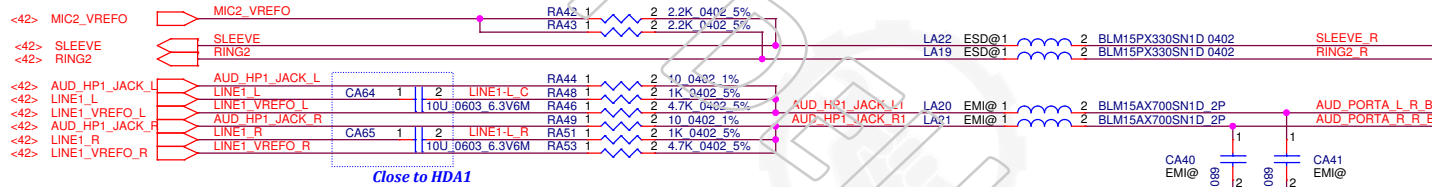
Main Func = Audio

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

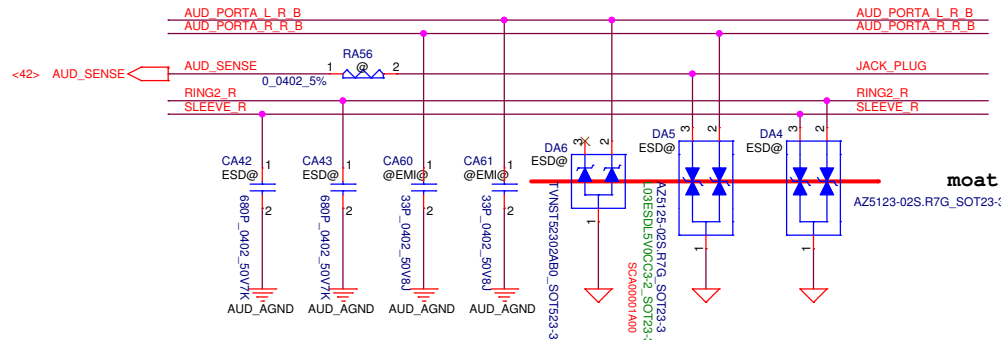


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

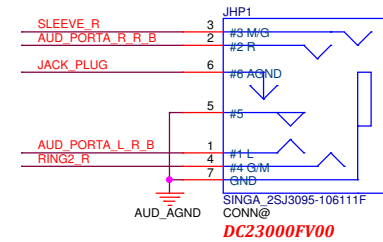


Close to HDA1

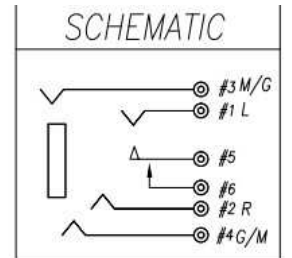
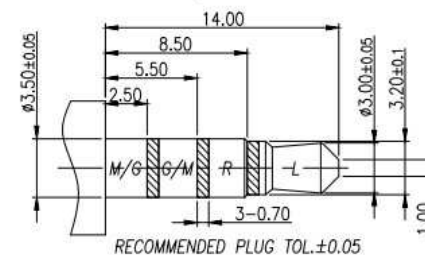
Universal Jack



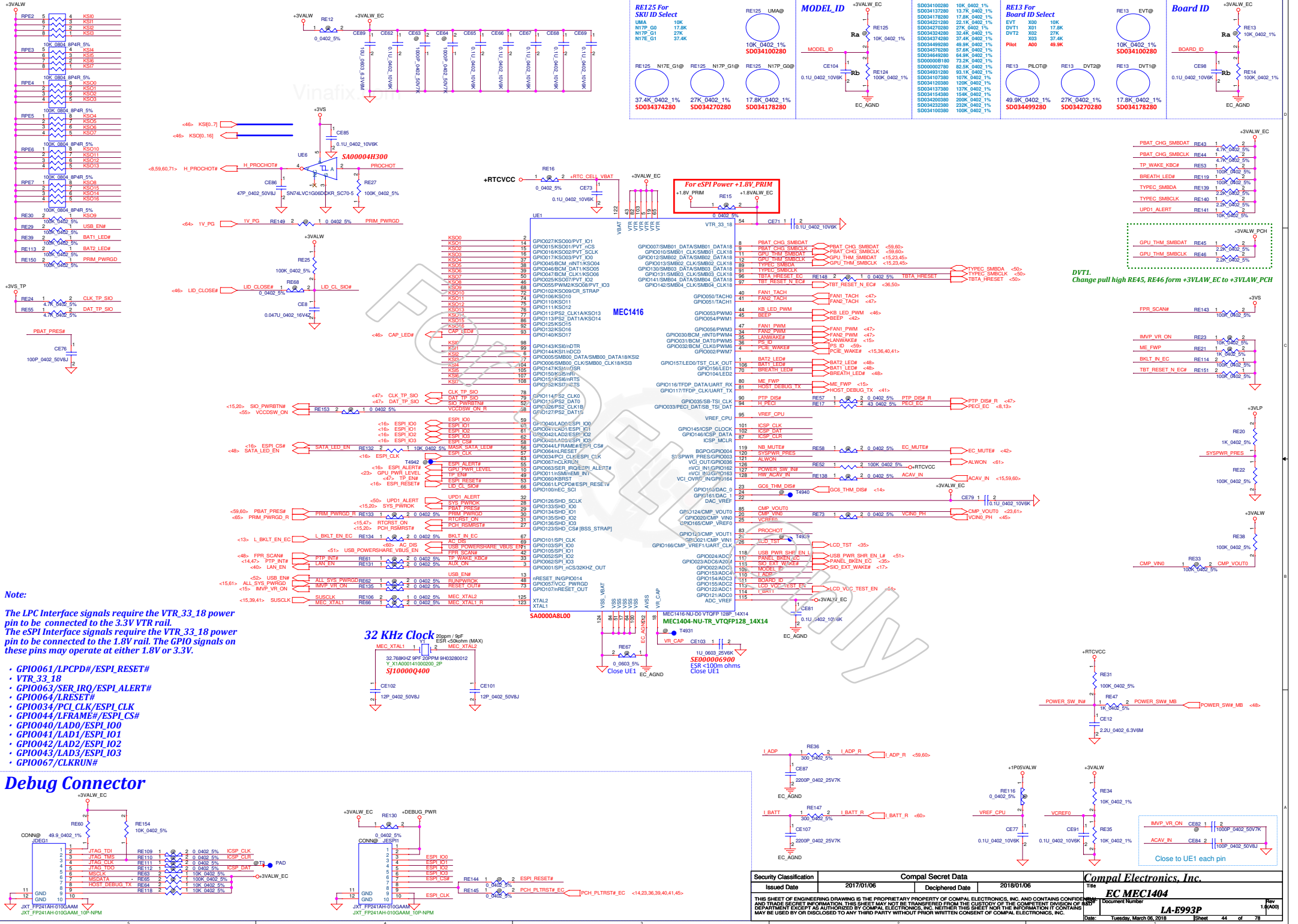
moat



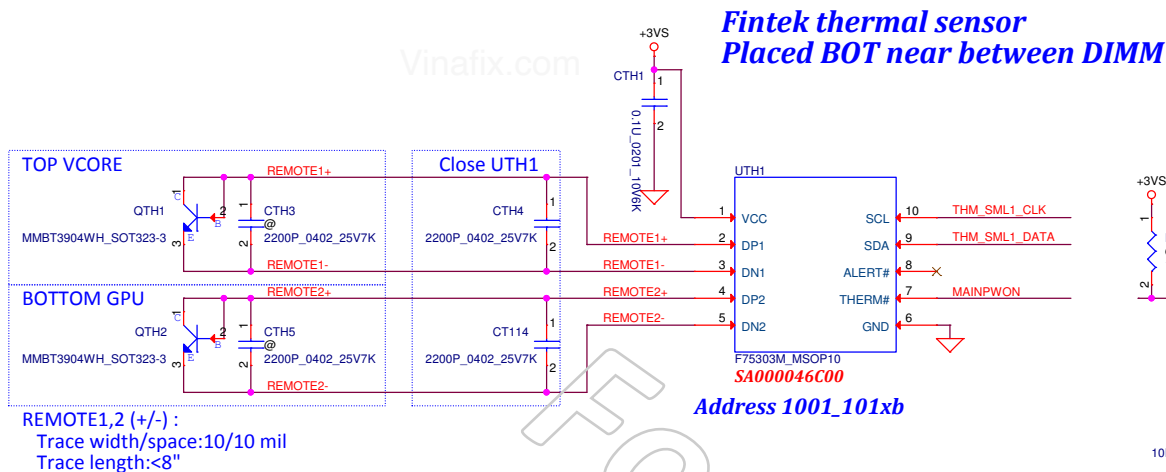
SINGA_2SJ3095-106111F



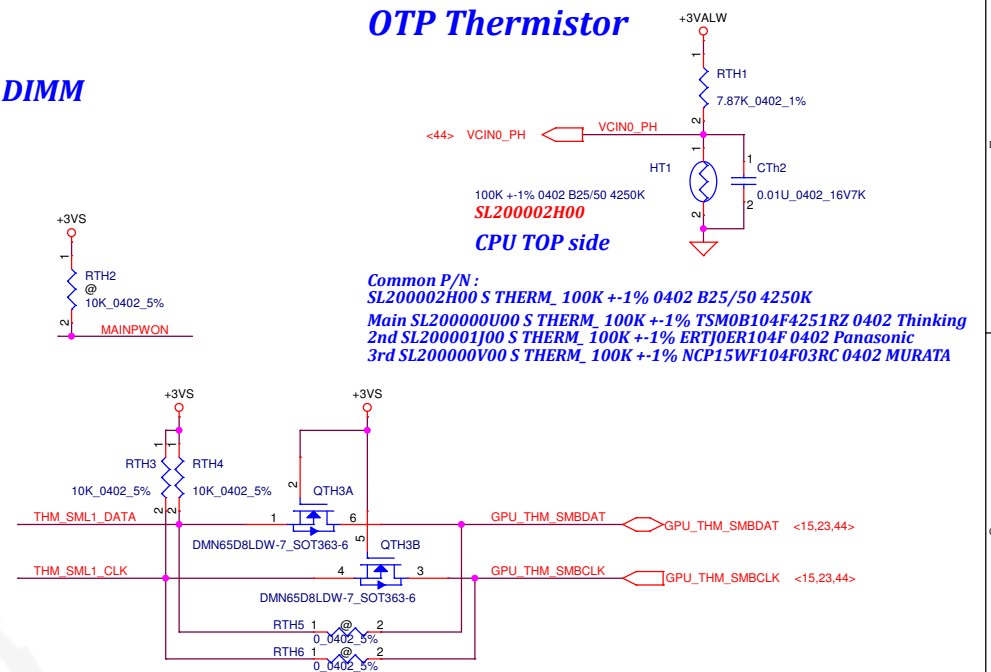
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Issued Date	2017/01/06	Deciphered Date	2018/01/06
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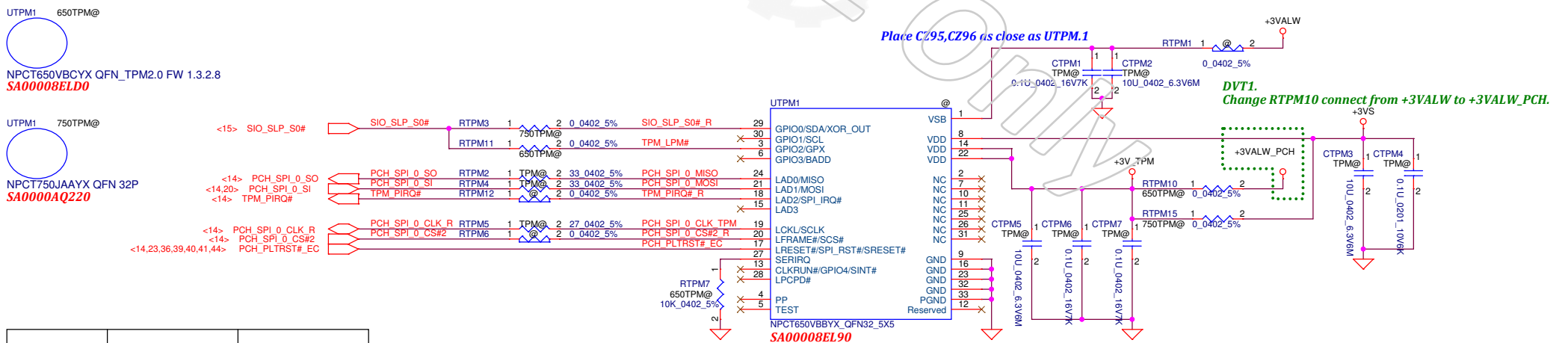
Thermal Sensor



OTP Thermistor



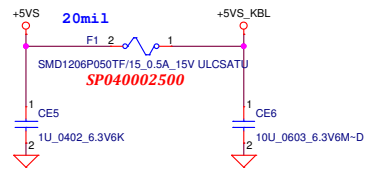
TPM



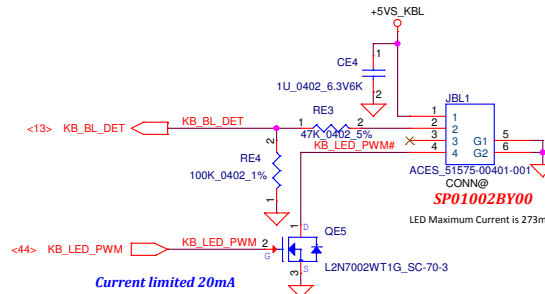
TPM Model	NPCT650VBCYX	NPCT750JAAYX
Pop	RTPM11 RTPM10 RTPM7	RTPM3 RTPM15
Un-pop	RTPM3 RTPM15	RTPM11 RTPM10 RTPM7

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								Document Number		LA-E993P		Rev 1.0(A00)	
								Date:		Tuesday, March 06, 2018		Sheet 45 of 78	

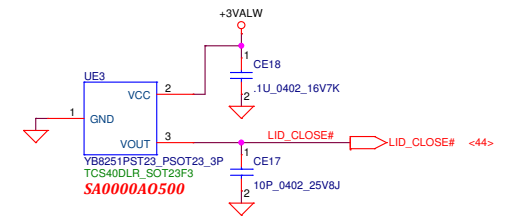
Fuse for KB Backlight



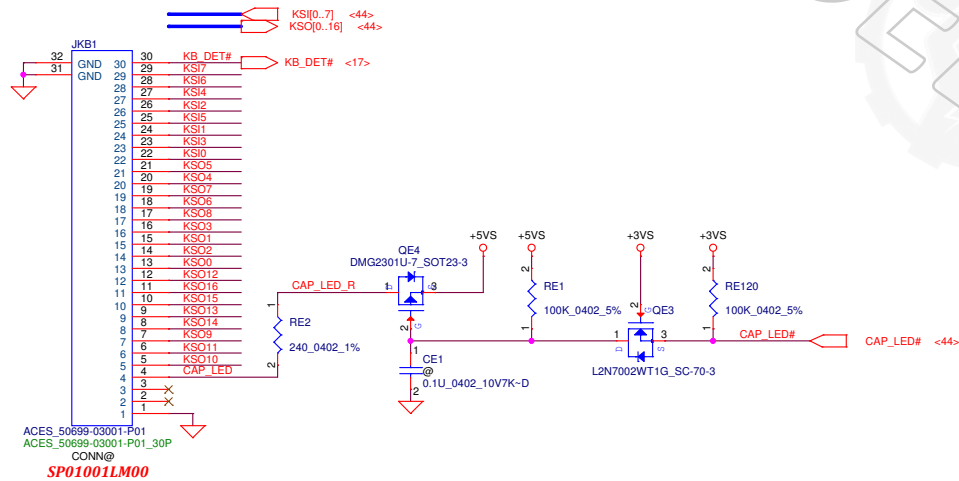
Connector for Keyboard Backlight



Lid Switch

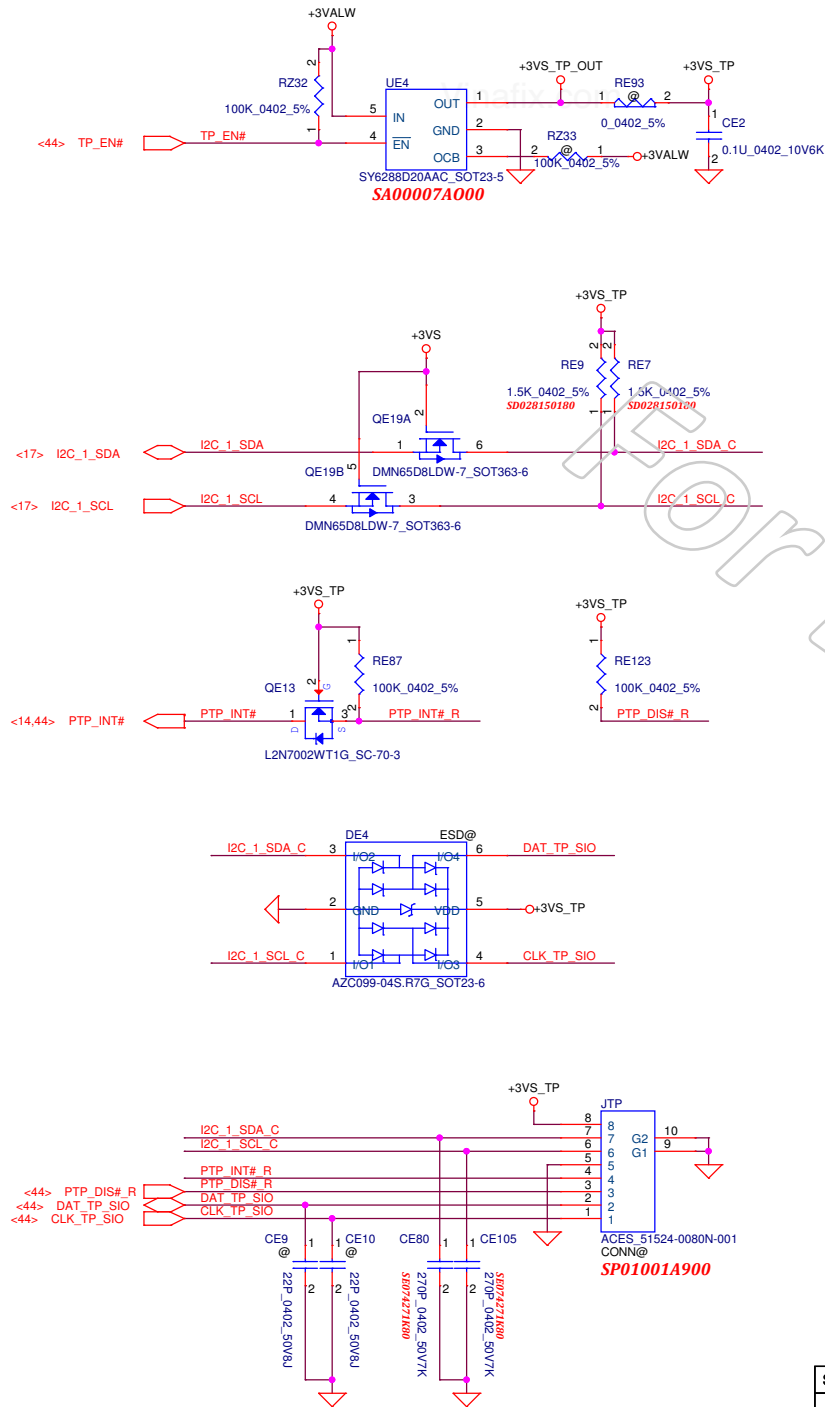


Connector for Keyboard

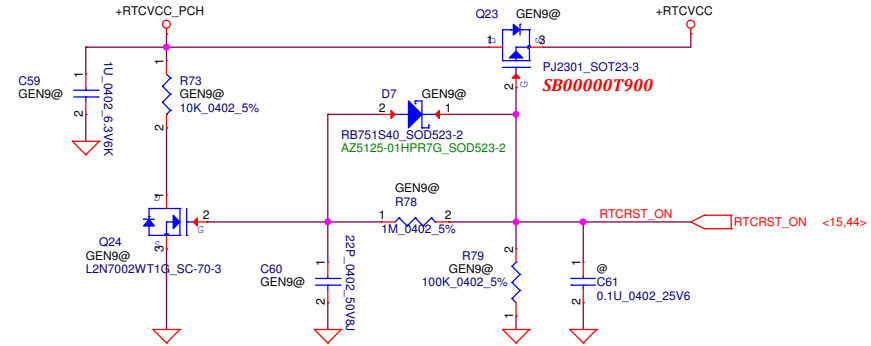


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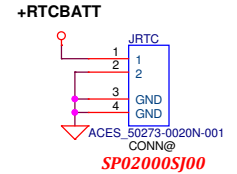
Touch pad



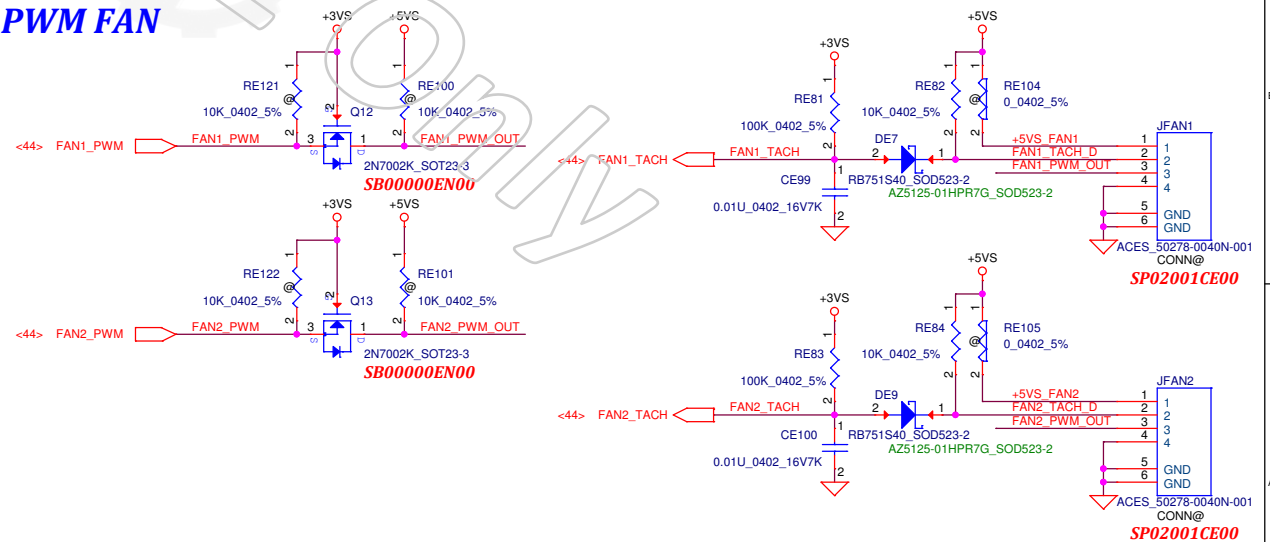
RTC GEN 9



RTC Battery

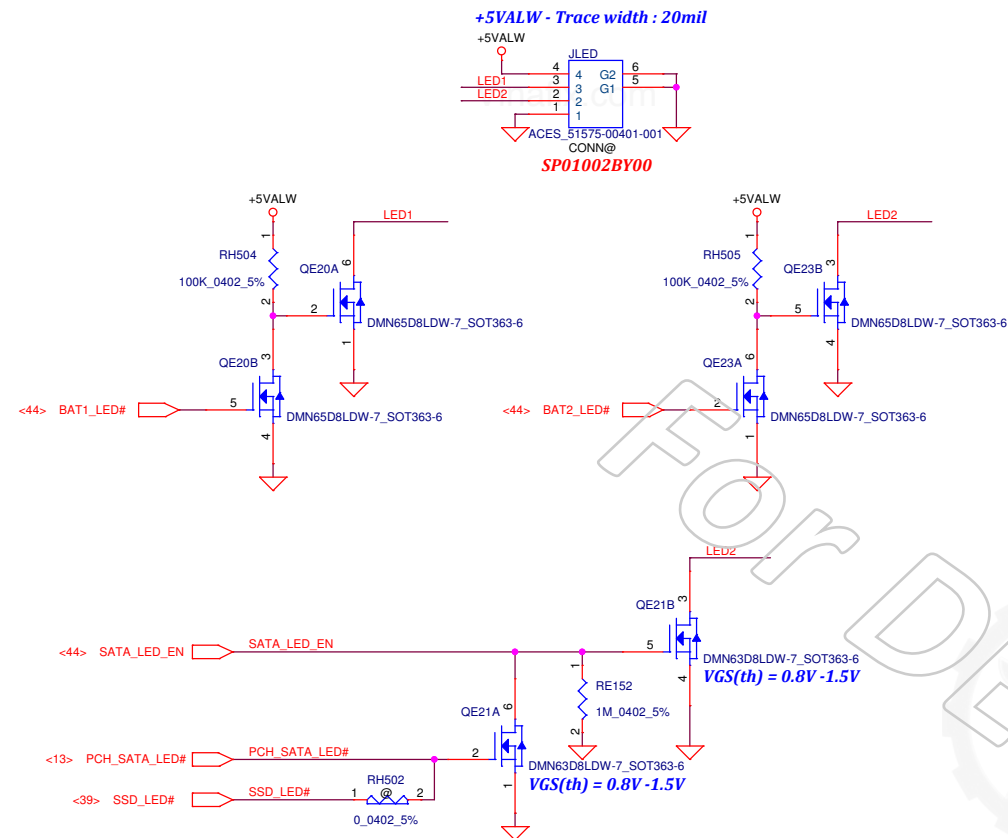


PWM FAN

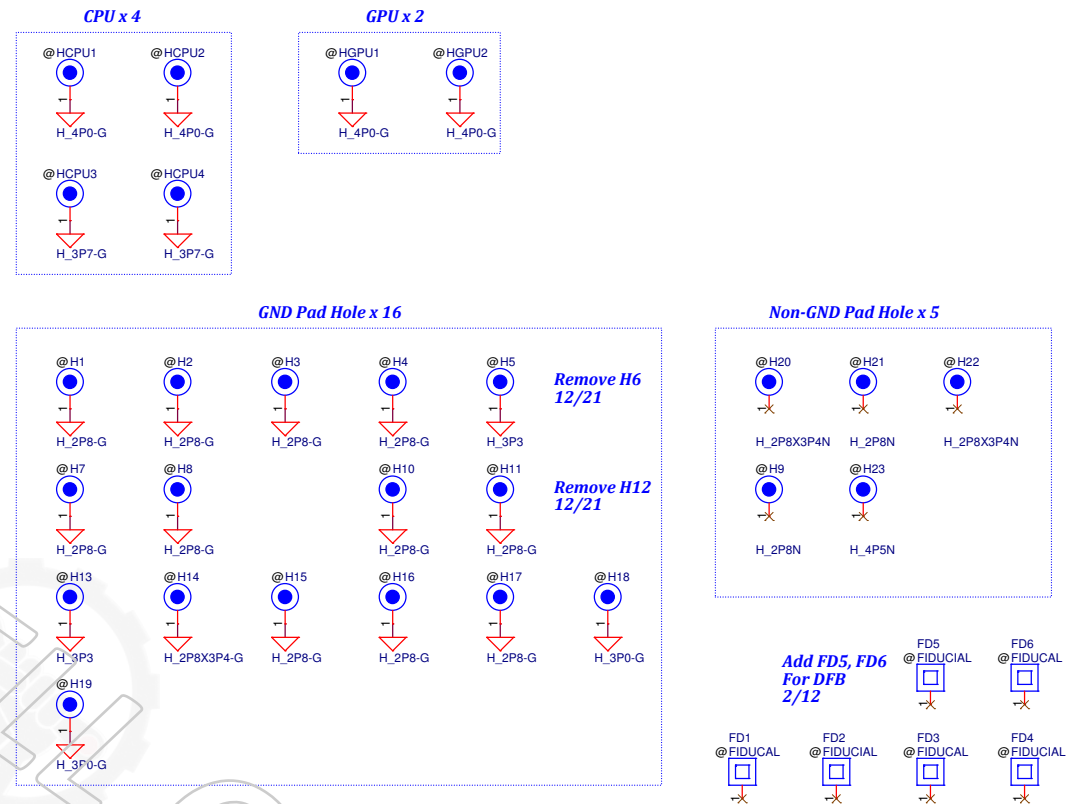


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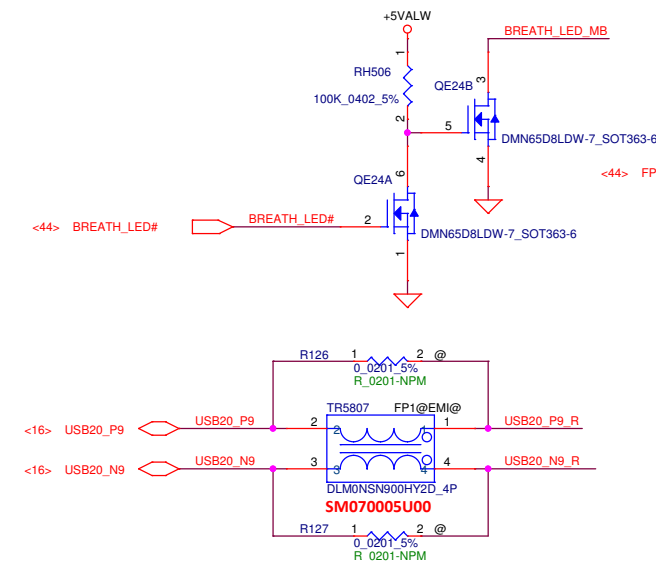
LED Board Connector



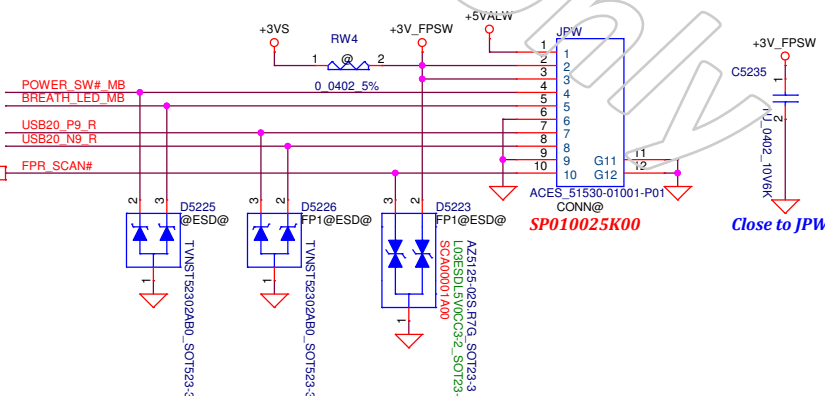
Screw Hole - Base on 0505 ME Drawing



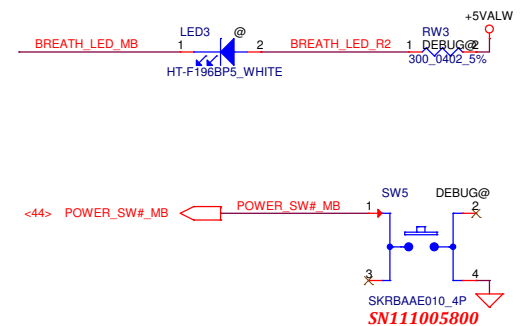
PWR BOARD Connector



Touch Finger Print module.



Power Button & LED (Reserve)

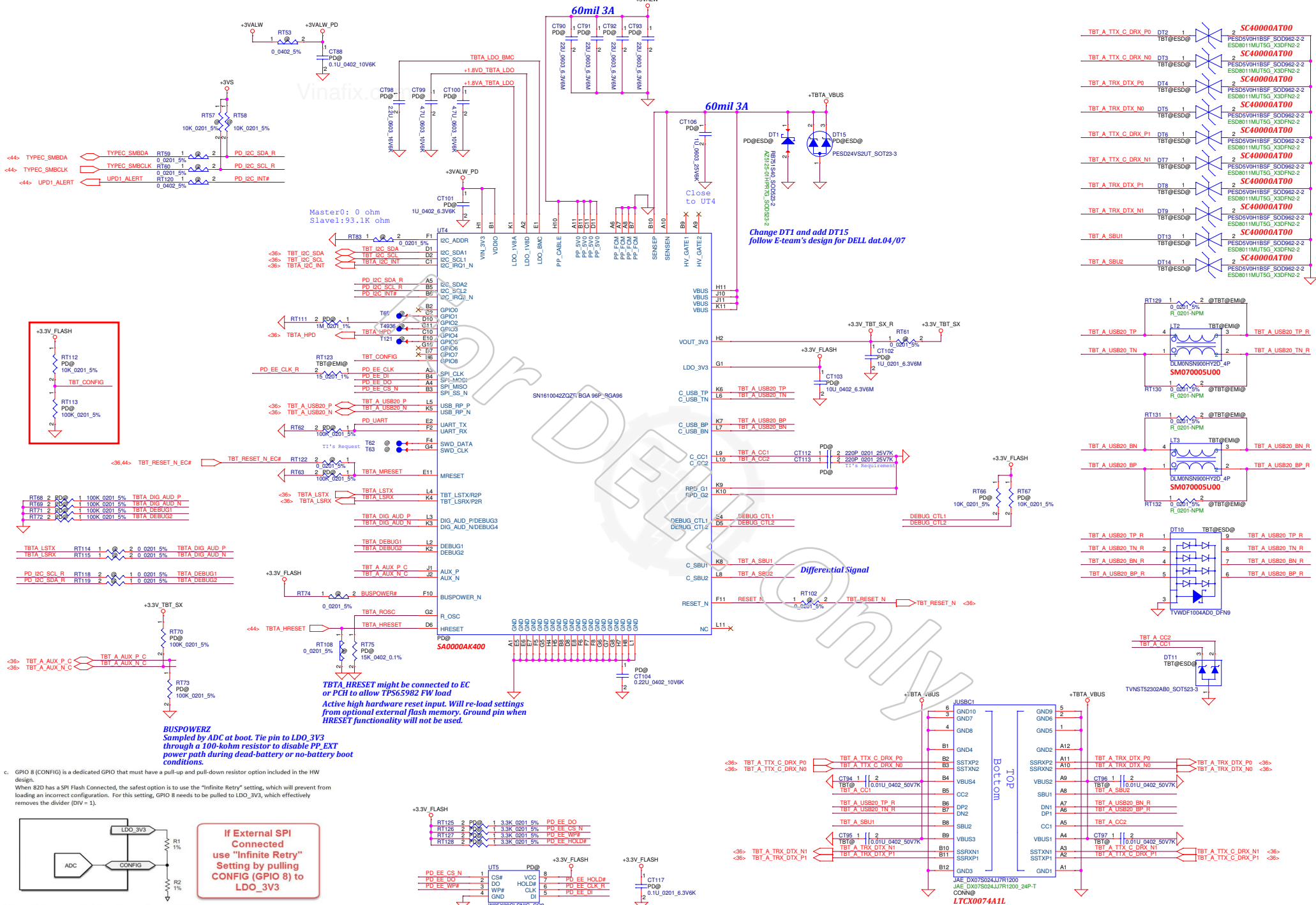


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CONN/LED/Screws/PW						Rev		
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						Size	Document Number	LA-E993P
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Reserved

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c. GPIO 8 (CONFIG) is a dedicated GPIO that must have a pull-up and pull-down resistor option included in the HW design. When S2D has a SPI Flash Connected, the safest option is to use the "Infinite Retry" setting, which will prevent from loading an incorrect configuration. For this setting, GPIO 8 needs to be pulled to LDO_3V3, which effectively removes the divider (DIV = 1).

TBTA HRESET might be connected to EC or PCH to allow TP565982 FW load
Active high hardware reset input. Will re-load settings from optional external flash memory. Ground pin when HRESET functionality will not be used.

BUSPOWERZ
Sampled by ADC at boot. Tie pin to LDO_3V3 through a 100-kohm resistor to disable PP_EXT power path during dead-battery or no-battery boot conditions.

If External SPI Connected use "Infinite Retry" Setting by pulling CONFIG (GPIO 8) to LDO_3V3

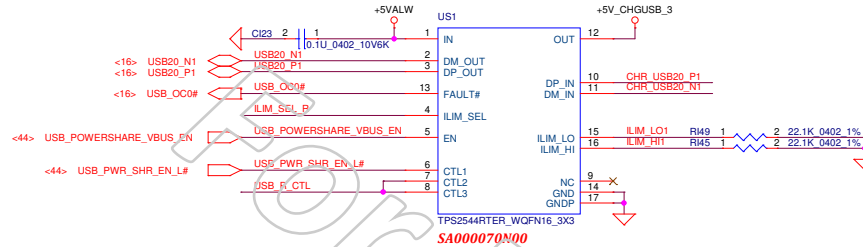
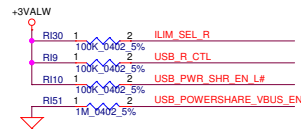
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				PD+USB3.1 type C	
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USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

USB3.0 / USB2.0 Port1



USB3.0 Re-driver

Setting Status							
		B_EQ		A_EQ		B_DE	
PI3EQX7502AI		NC	6.0dB	NC	6.0dB	NC	-3.5dB
		0	3.0dB	0	3.0dB	0	0.0dB
		1	9dB	1	9dB	1	-6.0dB
		A		B		A	
		EQ0EQ1	A_EQ	EQ0EQ1	B_EQ	DE0DE1	A_DE
PS8713		0 0	9.5dB	0 0	9.5dB	0 0	-3.5dB
		0 1	4.5dB	0 1	4.5dB	0 1	-2.7dB
		1 0	13 dB	1 0	13 dB	1 0	0.0dB
		1 1	7.5dB	1 1	7.5dB	1 1	-5.0dB

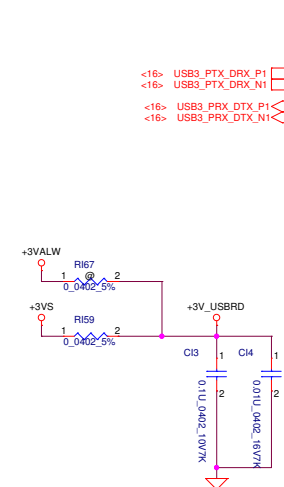
* red color is current setting

From PCH

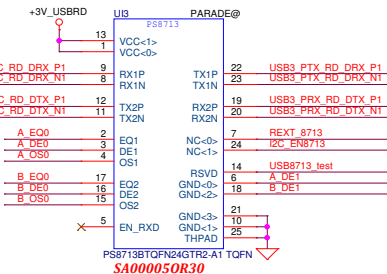
PERICOM: RXA, PS8713: B_In
PERICOM: TXB, PS8713: A_Out

To USB3 CONN

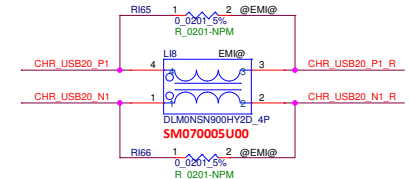
PERICOM: TXA, PS8713: B_Out
PERICOM: RXB, PS8713: A_In



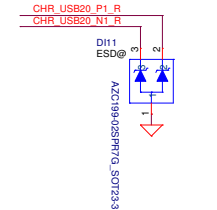
PI3EQX7502AI/DEX TOFN24 USB3.0 REDR
SA00006WV00



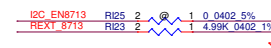
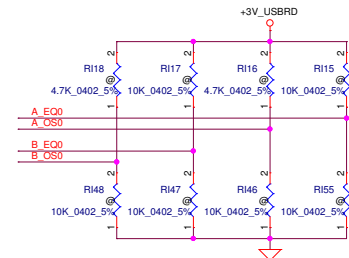
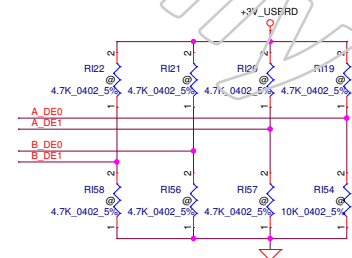
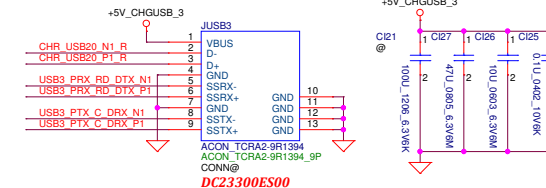
PS8713:
Pin8,9=B_In, P22,23=B_Out
Pin11,12=A_Out, Pin19,20=A_In
Pin 17=A_EQ0, Pin 15=A_EQ1
Pin 16=A_DE0, Pin 18=A_DE1
Pin 2=B_EQ0, Pin 4=B_EQ1
Pin 3=B_DE0, Pin 6=B_DE1



Place close to USB3

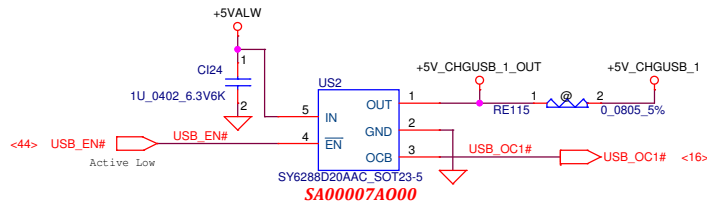


USB3.0 / USB2.0 Left Side



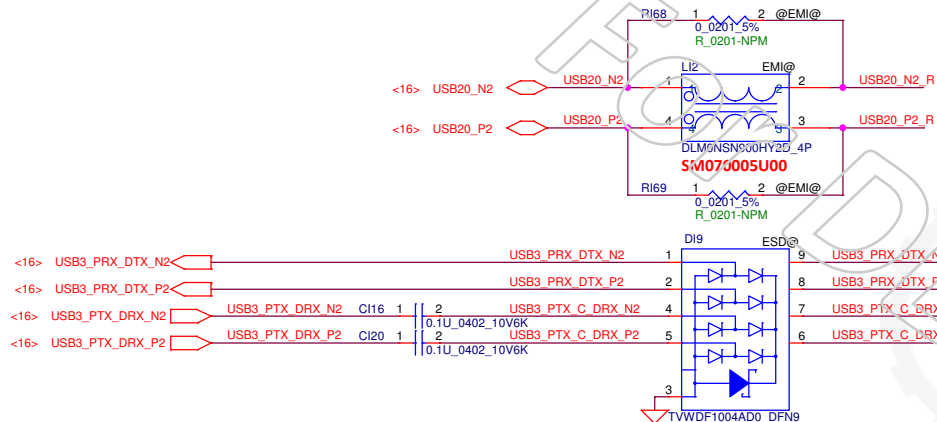
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USB Power Switch

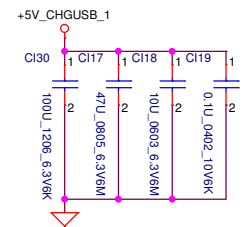
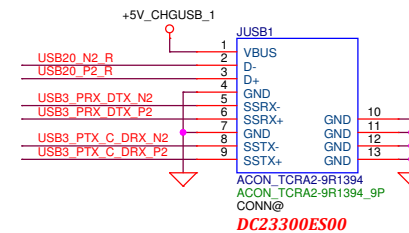
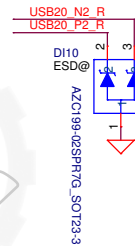


+5VALW
+5V_CHGUSB_1
+5V_CHGUSB_1_OUT
 Trace width : 100mil

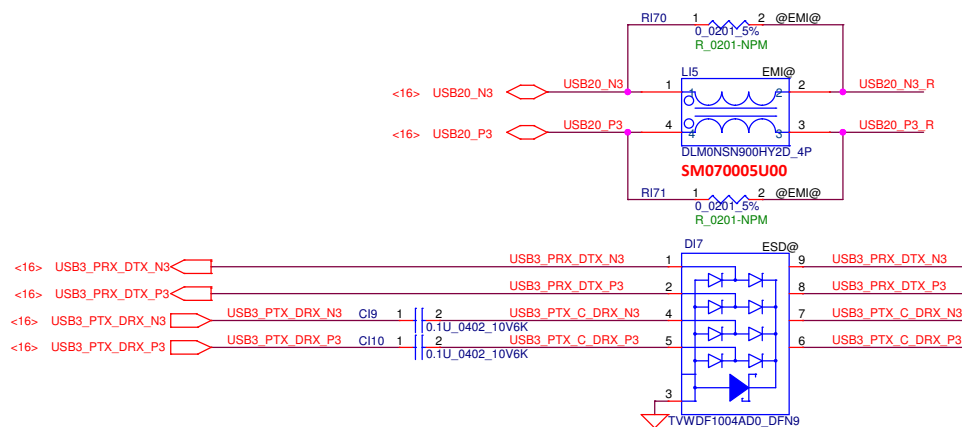
USB3.0 / USB2.0 Right Side



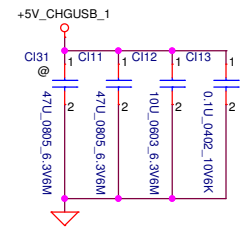
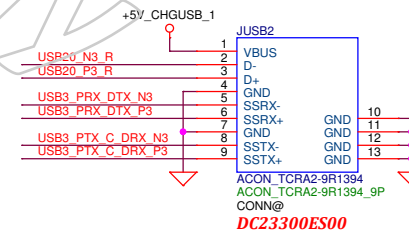
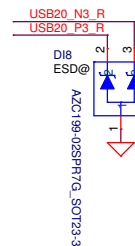
Place close to JUSB1



USB3.0 / USB2.0 Right Side



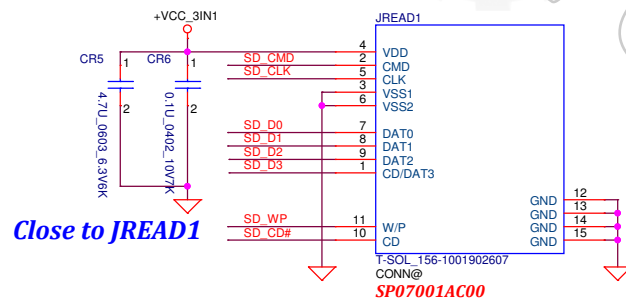
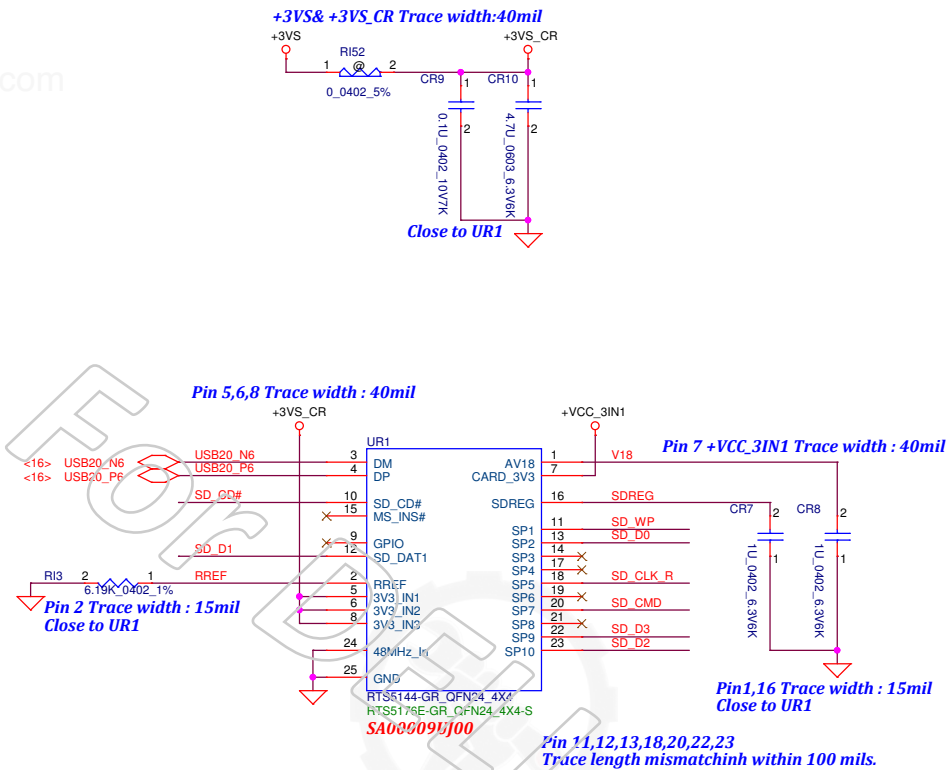
Place close to JUSB2



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Card Reader

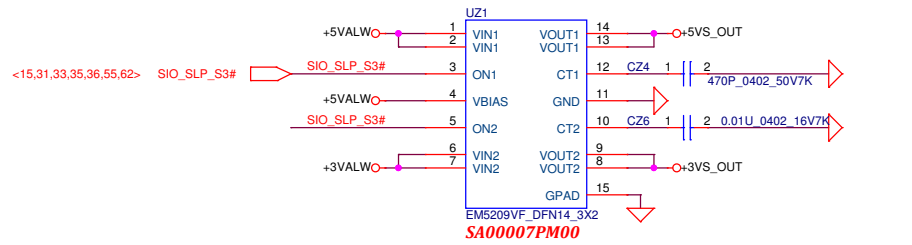
Vinafix.com



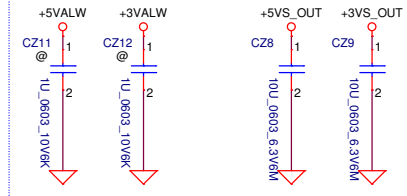
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+5VALW to +5VS +3VALW to +3VS

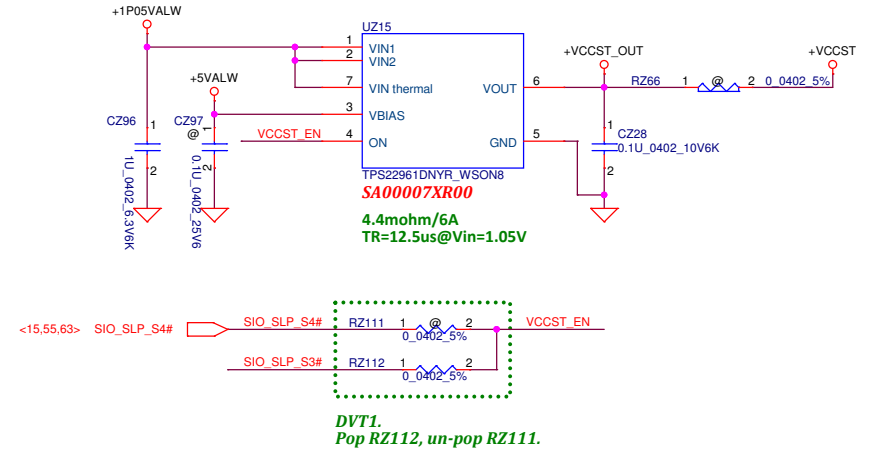
Vinafix.com



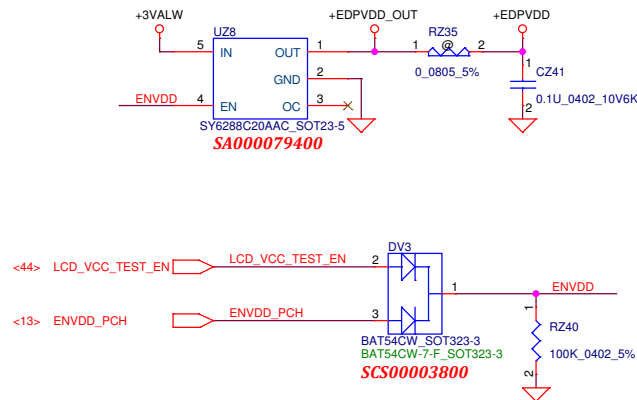
Close UZ1



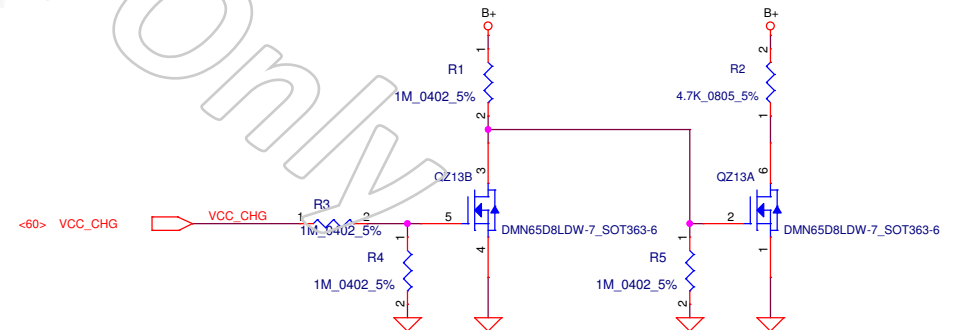
+VCCST Load Switch



eDP Load Switch

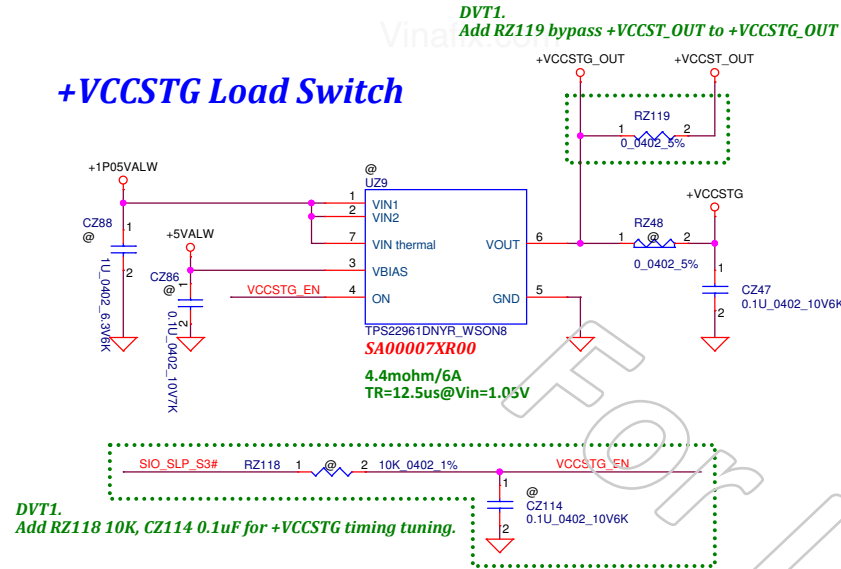


B+ Discharge



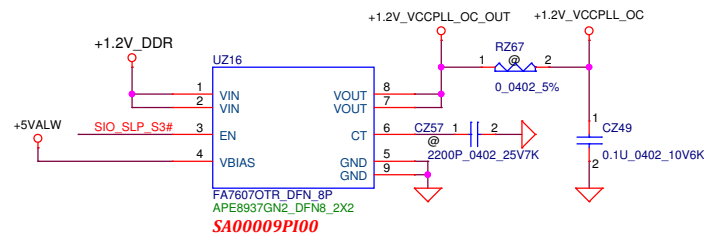
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/01/06	Deciphered Date	2018/01/06	Title	SYS DC/DC Interface
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-E993P
				Date:	Tuesday, March 06, 2018
				Sheet	54 of 78

+VCCSTG Load Switch

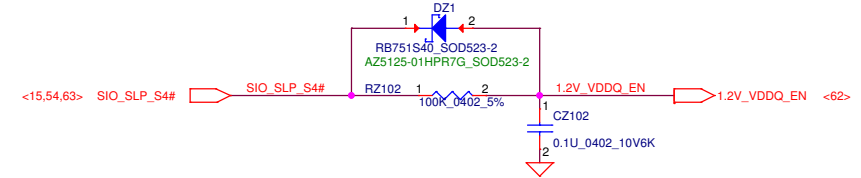


+VCCPLL_OC Load Switch

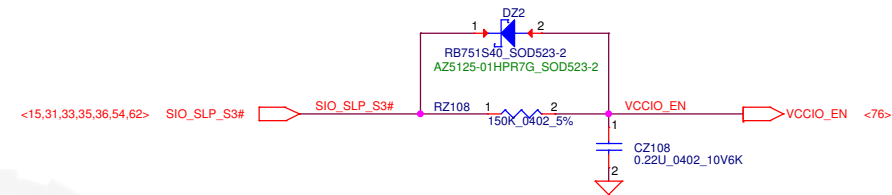
H-Processor Line - Quad Core GT2
Max : 130 mA



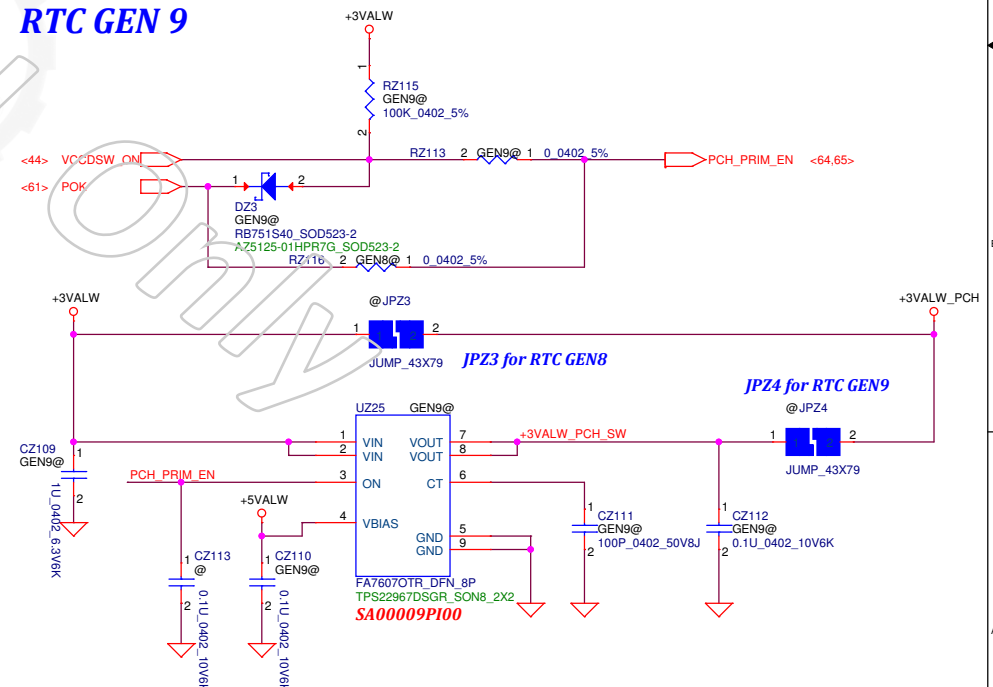
+1.2V_DDR Enable



+VCCIO Enable



RTC GEN 9



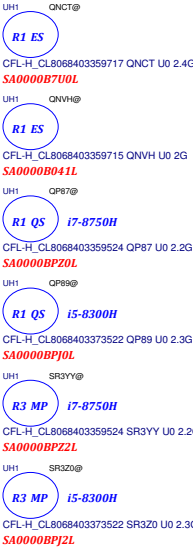
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/01/06	Deciphered Date	2018/01/06	Title	DC/DC/S0iX/CS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-E993P
				Date	Tuesday, March 06, 2018
				Sheet	55 of 78

MODEL NAME : DDK51/ DDK52/ DDK53

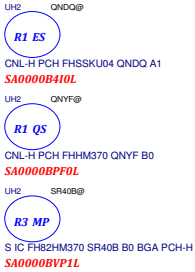
PCB NO : LA-E993P

Bom Structure

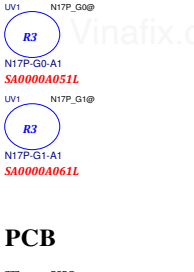
CPU



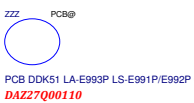
PCH



GPU

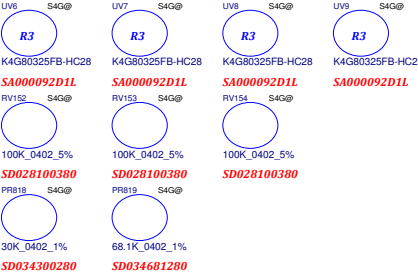


PCB



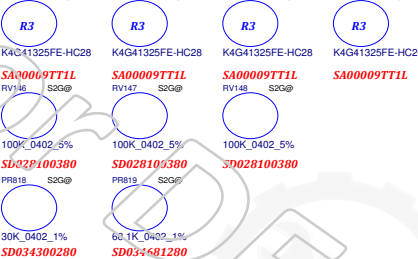
X76 : S4G@X7673331L54

Samsung 4G



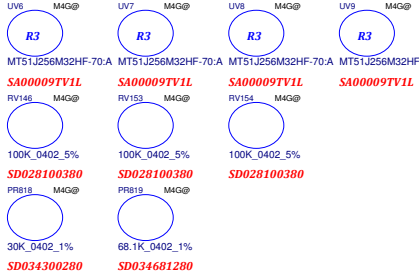
X76 : S2G@X7673331L51

Samsung 2G



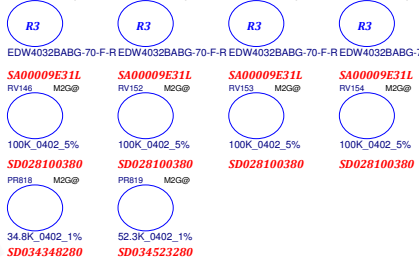
X76 : M4G@ X7673331L56

Micron 4G



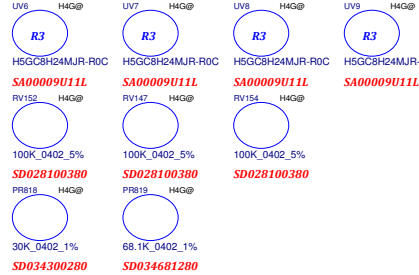
X76 : M2G@X7673331L53

Micron 2G



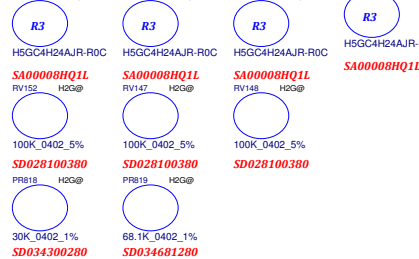
X76 : H4G@X7673331L55

Hynix 4G



X76 : H2G@X7673331L52

Hynix 2G



X43		Firestar/Firestar-B								Armani							
		431A9U31101	431A9U31102	431A9U31103	431A9U31104	431A9U31151	431A9U31152	431A9U31153	431A9U31154	431A9U31101	431A9U31102	431A9U31103	431A9U31104	431A9U31151	431A9U31152	431A9U31153	431A9U31154
PCB	PCB@																
Project ID	AMN@																
CPU ES 2.4G	QNCT@																
CPU ES 2.0G	QNVH@																
CPU QS 17-8750H	QP87@																
CPU QS 15-8300H	QP89@																
CPU MP 17-8750H	SR3YY@																
CPU MP 15-8300H	SR3Z@																
PCH	QNDQ@																
	QNYF@																
	SR40B@																
GPU ID	UMA@																
	N17P_G0@																
	N17P_G1@																
	N17E_G1@																
GPU	N17P@																
	EVT@																
	DVT1@																
	DVT2@																
Thunderbolt	PILOT@																
PD controller	TBT@																
HDMI2.0 re-timer	PD@																
CVI	CVI@																
RTC sequence	GEN@																
VGA	GEN@																
Free Fall sensor	VGA@																
	FFS@																
TPM	TPM@																
With TPM	650TPM@																
	750TPM@																
w/o TPM	NON_TPM@																
USB3.0 redriver	PERICOM@																
Touch screen	TS@																
XDP debug	XDP@																
On board switch	DEBUG@																
Connector	CONN@																
EMI/ESD/RF	X4E																
VRAM Option	X76																
Reserved, un-pop	@																
Reserved, un-pop	@PS8409@																

X4E		Firestar	Armani
Finger Print	FP1@EMI@		
General EMI	FP1@ESD@		
General ESD	EMI@		
TBT	TBT@EMI@		
TPS65982D	PD@ESD@		
Touch Screen	TS@EMI@		
RF	RF@		
VGA EMI	VGA@EMI@		
993 PCH SPI CLK	993@EMI@		
994 PCH SPI CLK	994@EMI@		
RF Reserve, un-pop	@RF@		
EMI Reserve, un-pop	@EMI@		
ESD Reserve, un-pop	@ESD@		
TS Reserve, un-pop	@TS@EMI@		
TBT Reserve, un-pop	@TBT@EMI@		
TBT Reserve, un-pop	@TBT@ESD@		

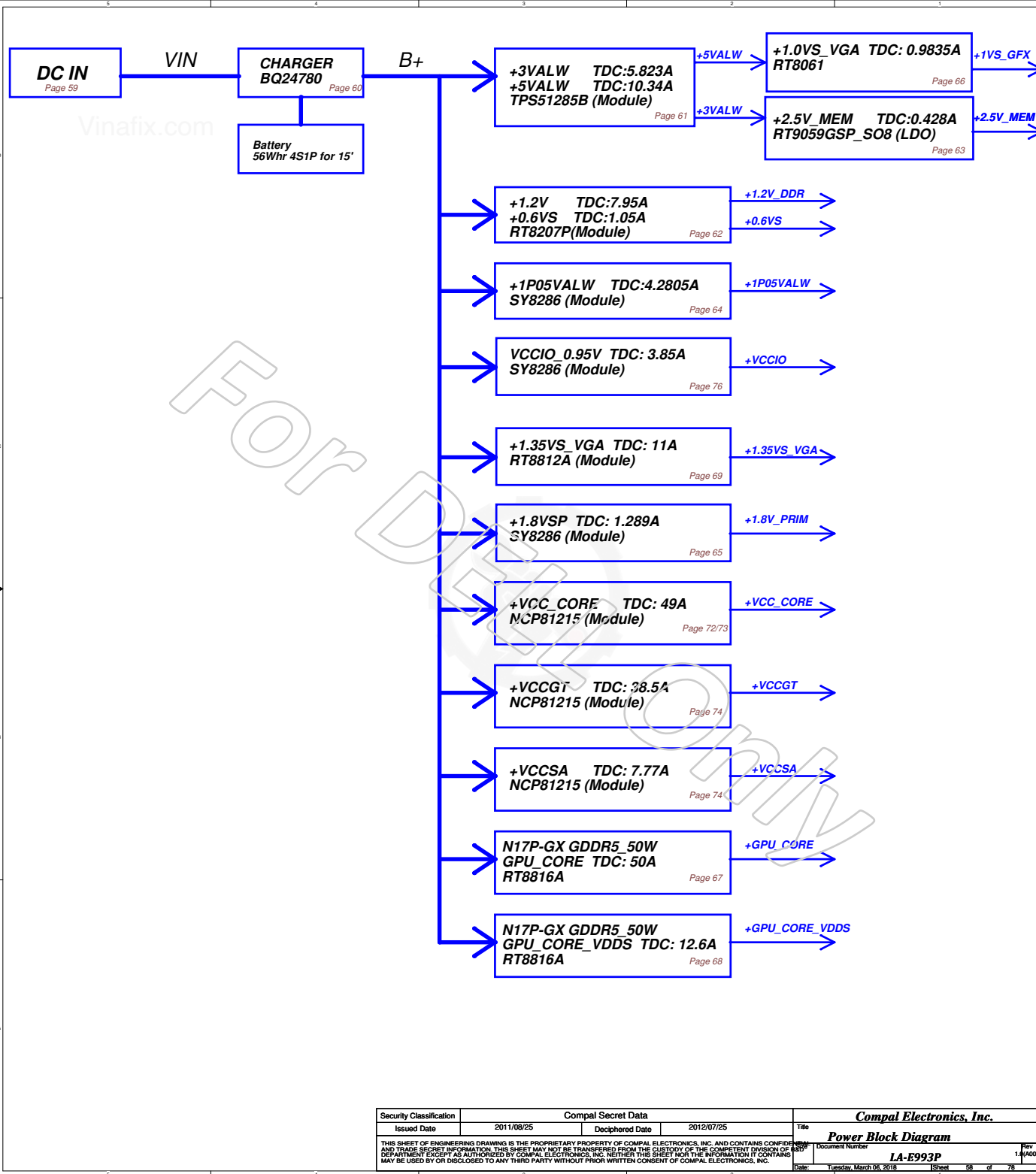
BOM config	GPU type	VRAM memory	VRAM vender	RVL	PR18	PR19
X7673331L51	N17P-G0/G1	128Mx32	Samsung	1.35V & 1.5V	30K	68.1K
X7673331L52	N17P-G0/G1	128Mx32	Hynix	1.35V & 1.5V	30K	68.1K
X7673331L53	N17P-G0/G1	128Mx32	Micron	1.35V & 1.55V	34.8K	52.3K
X7673331L54	N17P-G0/G1	256Mx32	Samsung	1.35V & 1.5V	30K	68.1K
X7673331L55	N17P-G0/G1	256Mx32	Hynix	1.35V & 1.5V	30K	68.1K
X7673331L56	N17P-G0/G1	256Mx32	Micron	1.35V & 1.5V	30K	68.1K

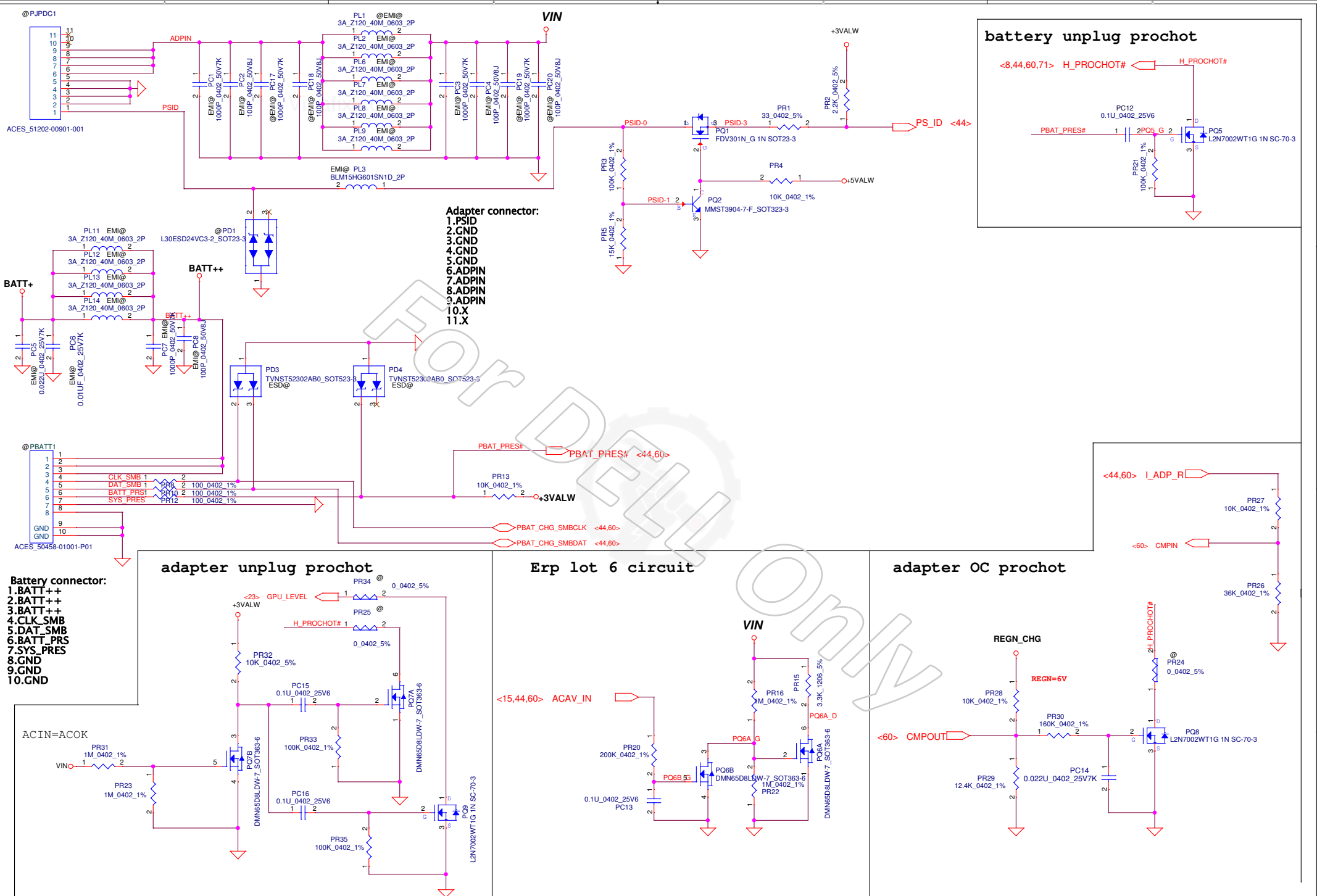
Security Classification		Compal Secret Data		Title	
Issued Date	2017/01/06	Deciphered Date	2018/01/06	NOTE	
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				LA-E993P	1.0/000
				Date: Tuesday, March 06, 2018	Sheet 56 of 78

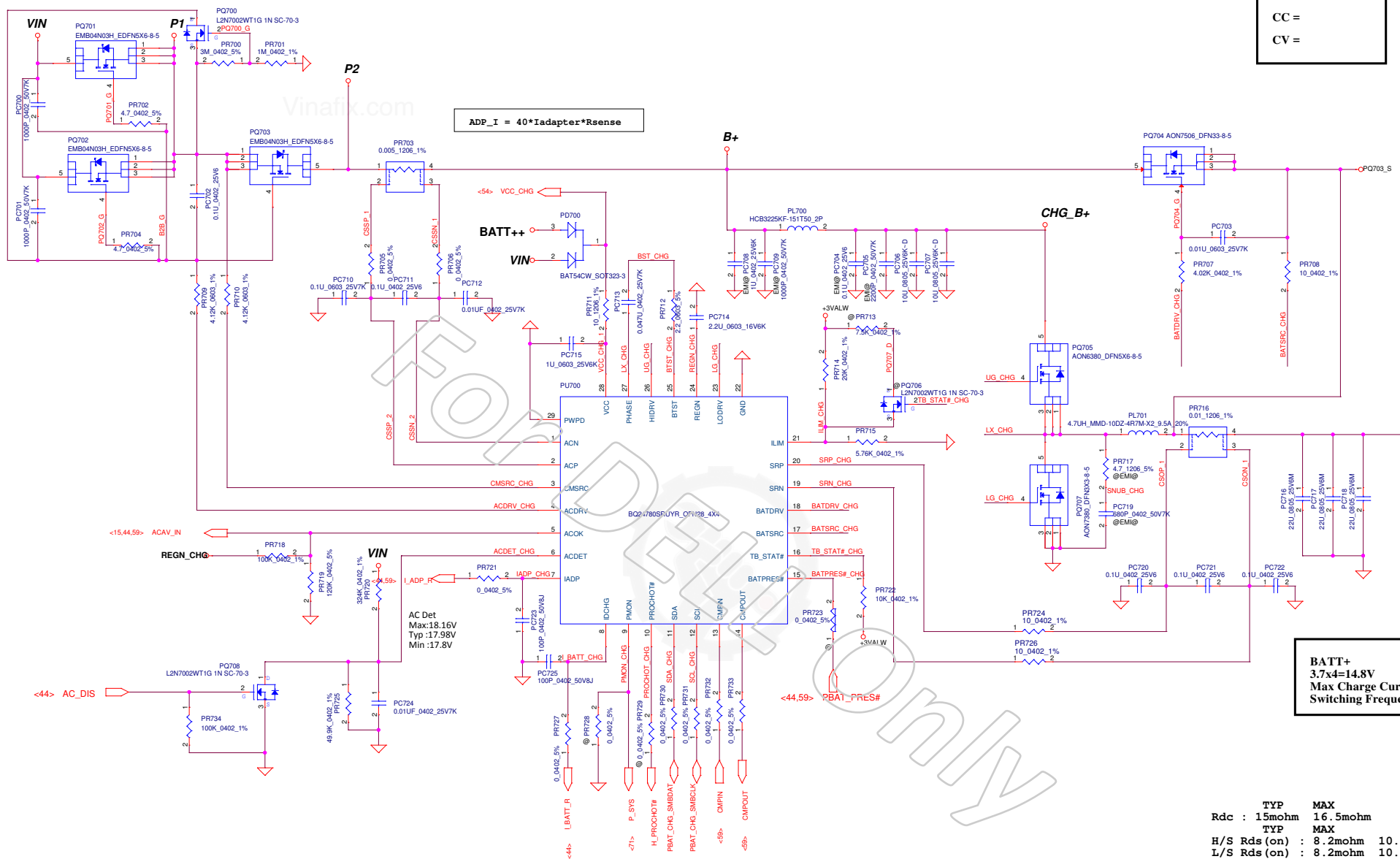
Vinafix.com

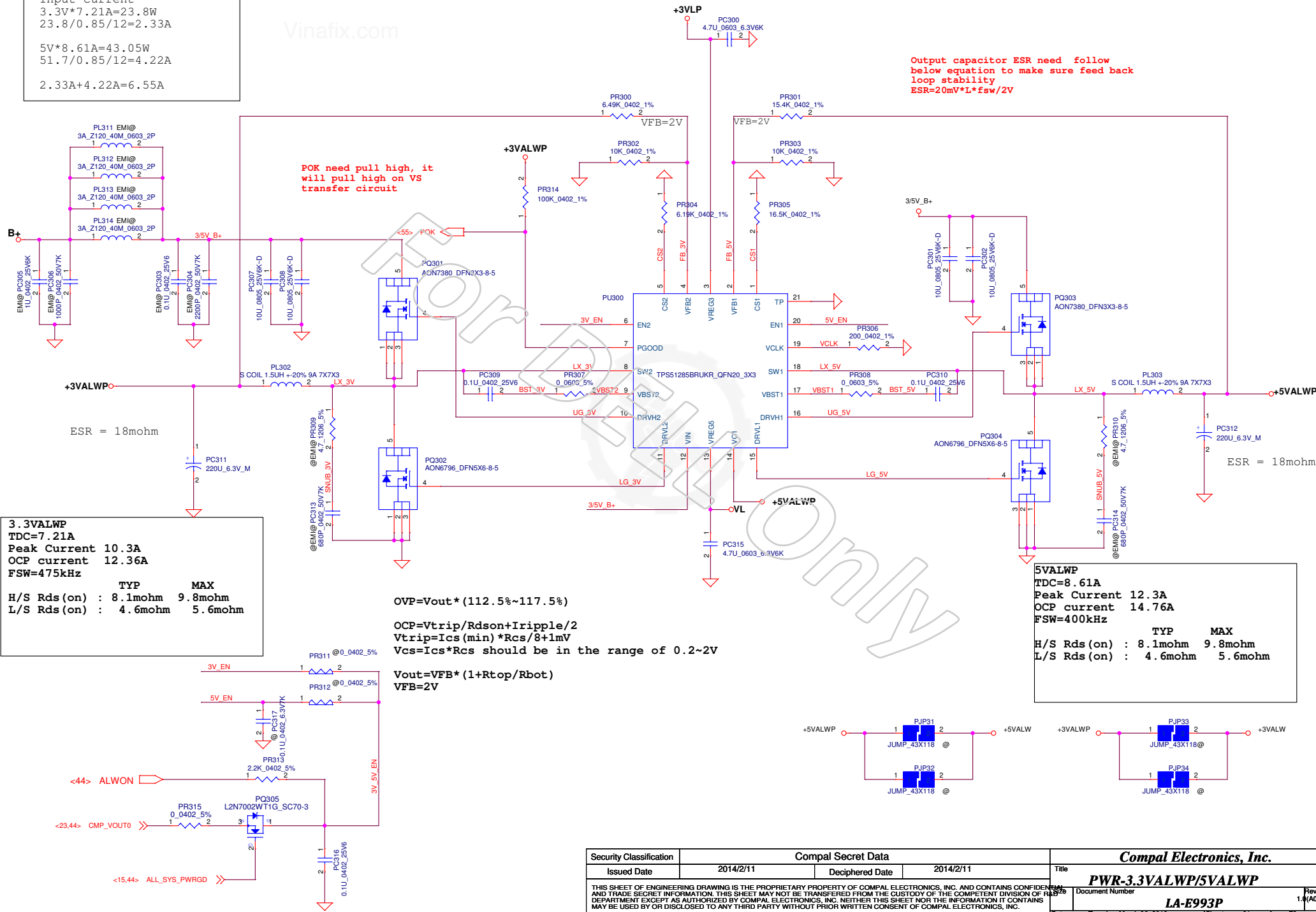
For DELL Only

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/01/06	Deciphered Date	2018/01/06	Title	NOTE
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				Date	Tuesday, March 06, 2018

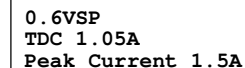






$$5V \cdot 8.61A = 43.05W$$
$$51.7 / 0.85 / 12 = 4.22A$$
$$2.33A + 4.22A = 6.55A$$


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	PWR-3.3VALWP/SVALWP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RA 726 DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-E993P	Rev 1.4/000
				Date:	Tuesday, March 06, 2018	Sheet 61 of 76

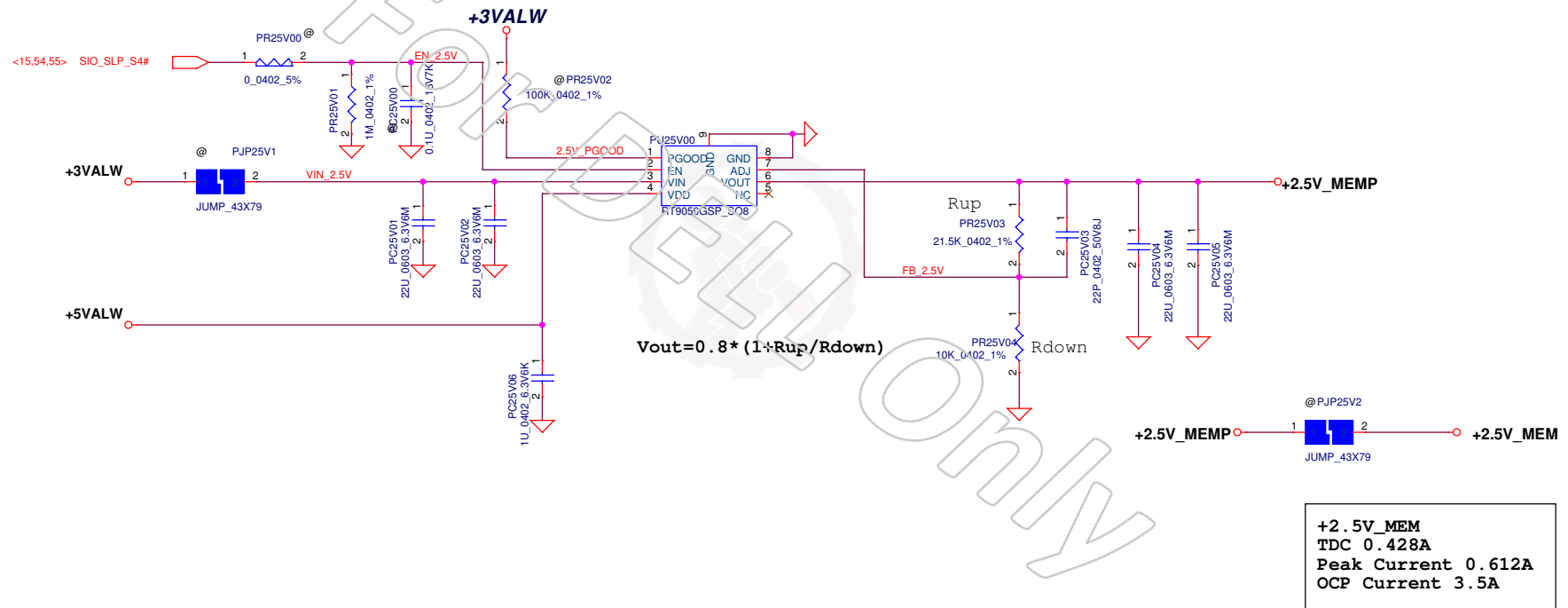

$$\text{RLIMIT} = \text{ILIMIT} \cdot R_{\text{on}} / 10 \mu\text{A}$$

where $\text{RI LMT} = \text{PR201} = 20.5 \text{K}$, $R_{\text{on}} = 15.8 \text{m}$
 $\Rightarrow \text{ILIMIT} = 15 \text{A}$

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/09/18	Deciphered Date	2016/09/18	Title	PWR-1.2VP/0.6VSP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					LA-E993P
Date:		Tuesday, March 06, 2018		Sheet	62 of 78

Input Current: 0.42A

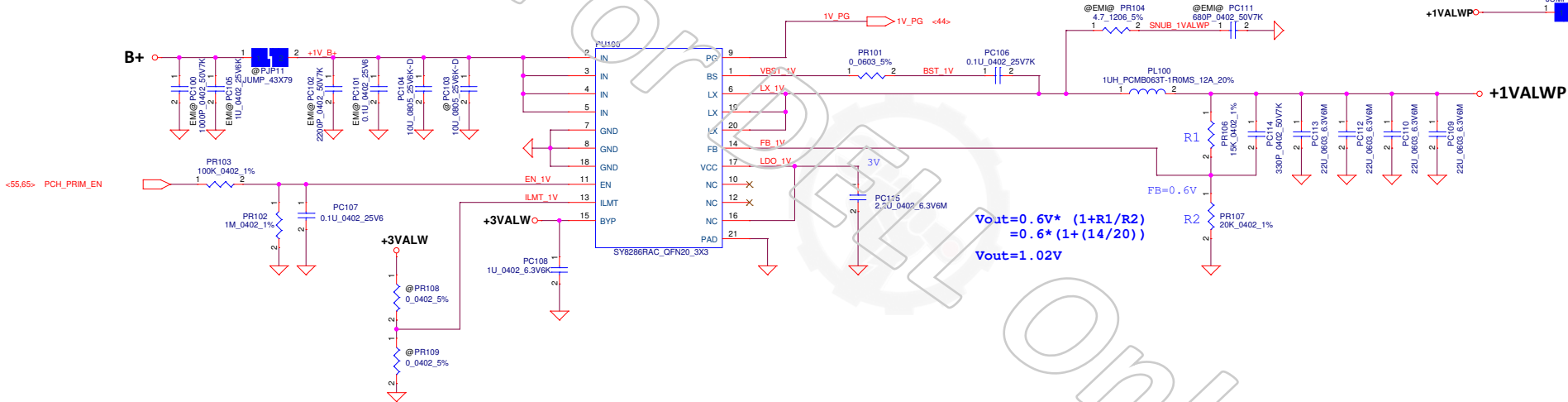
$2.5 \times 0.428 = 1.07W$
 $1.07 / 0.85 / 5 = 0.42A$



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/09/18	Deciphered Date	2016/09/18	Title	PWR +2.5V_MEM
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date	Tuesday, March 06, 2018
				Sheet	63 of 78
				Rev	1.0(A00)

IL=1.9A@19.5V
ripple=7.3mV@19.5V

+1VALWP 1 2 +1P05VALW



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

$$\begin{aligned} V_{out} &= 0.6V * (1 + R_1/R_2) \\ &= 0.6 * (1 + (14/20)) \\ V_{out} &= 1.02V \end{aligned}$$

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2015/09/18	Deciphered Date	2016/09/18	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF OUR DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev	
				LA-E993P		1.0(400)
				Date:	Tuesday, March 06, 2018	Sheet

Input Current: 0.318A

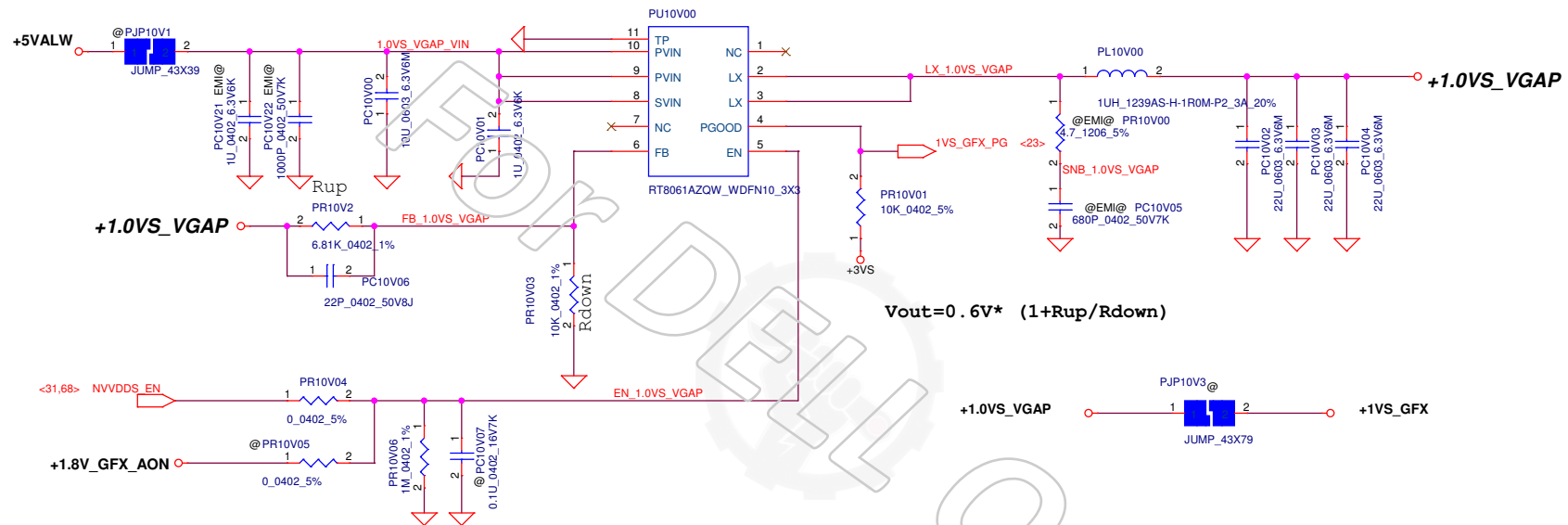
$1.8 \times 1.806 / 0.85 / 12V = 0.318A$

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

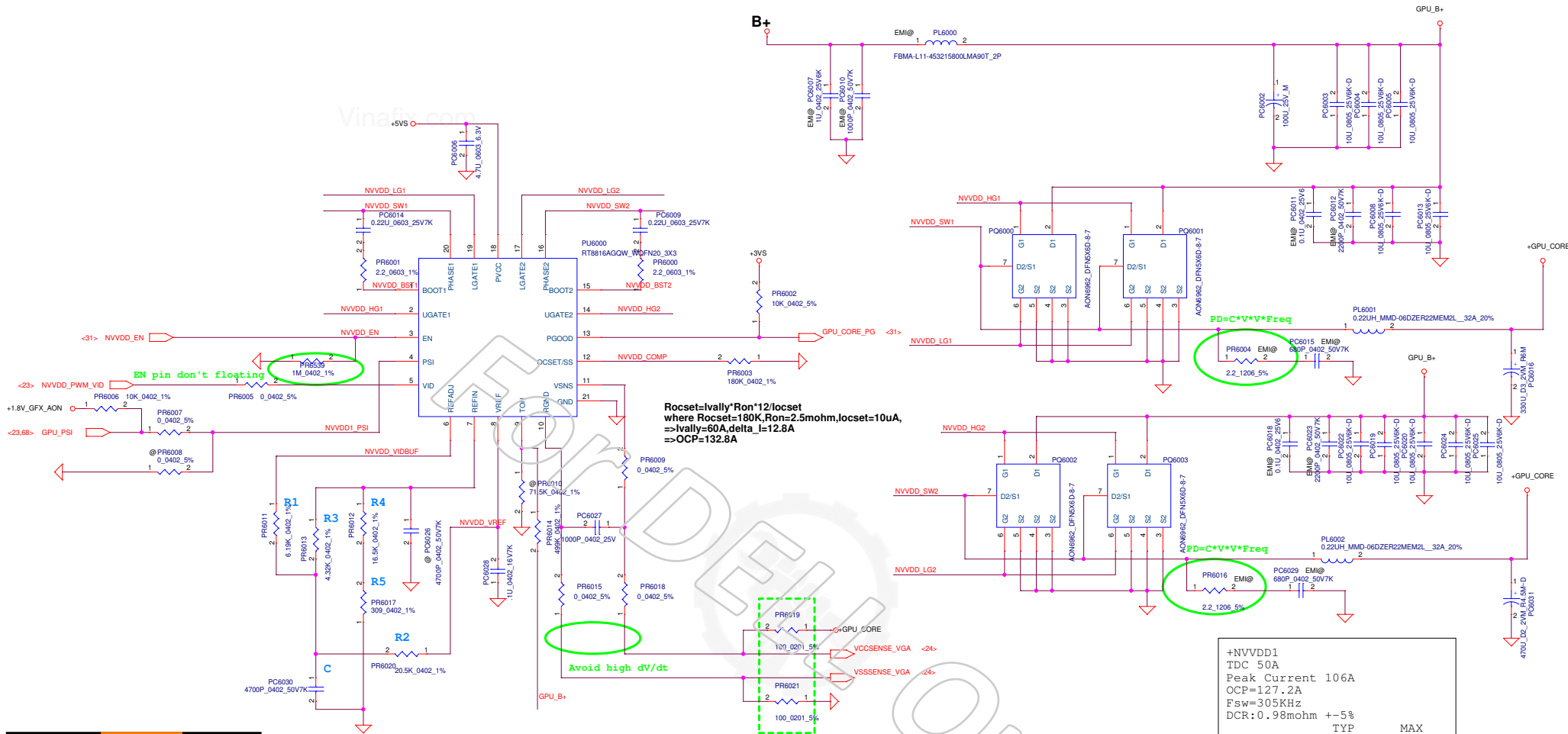
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR +1.8VSP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					LA-E993P	1.0 (A00)
				Date: Tuesday, March 06, 2018	Sheet 65 of 78	

$$1 \times 0.77 / 0.85 / 5 = 0.18 \text{ A}$$

```
+1.0VS_VGAP
TDC 0.77A
Peak Current 1.1A
OCP current 4A
FSW=1MHz
```



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR +1.0VS VGA
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				Date: Tuesday, March 06, 2018	Sheet 66 of 78

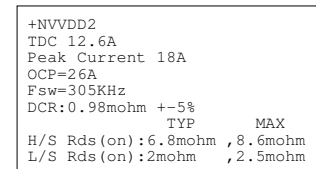


	2Phase DEM	2Phase CCM
PSI	1.22V	1.72V
PR6006	10Kohm	10Kohm
PR6228+PR6230	21Kohm	215Kohm

Operation Phase Number PSI Voltage Setting
 1phase with DEM 0V to 0.4V
 1phase with CCM 0.7V to 0.88V
 2phase with DEM 1.06V to 1.35V
 2phase with CCM 1.6V to 5.5V

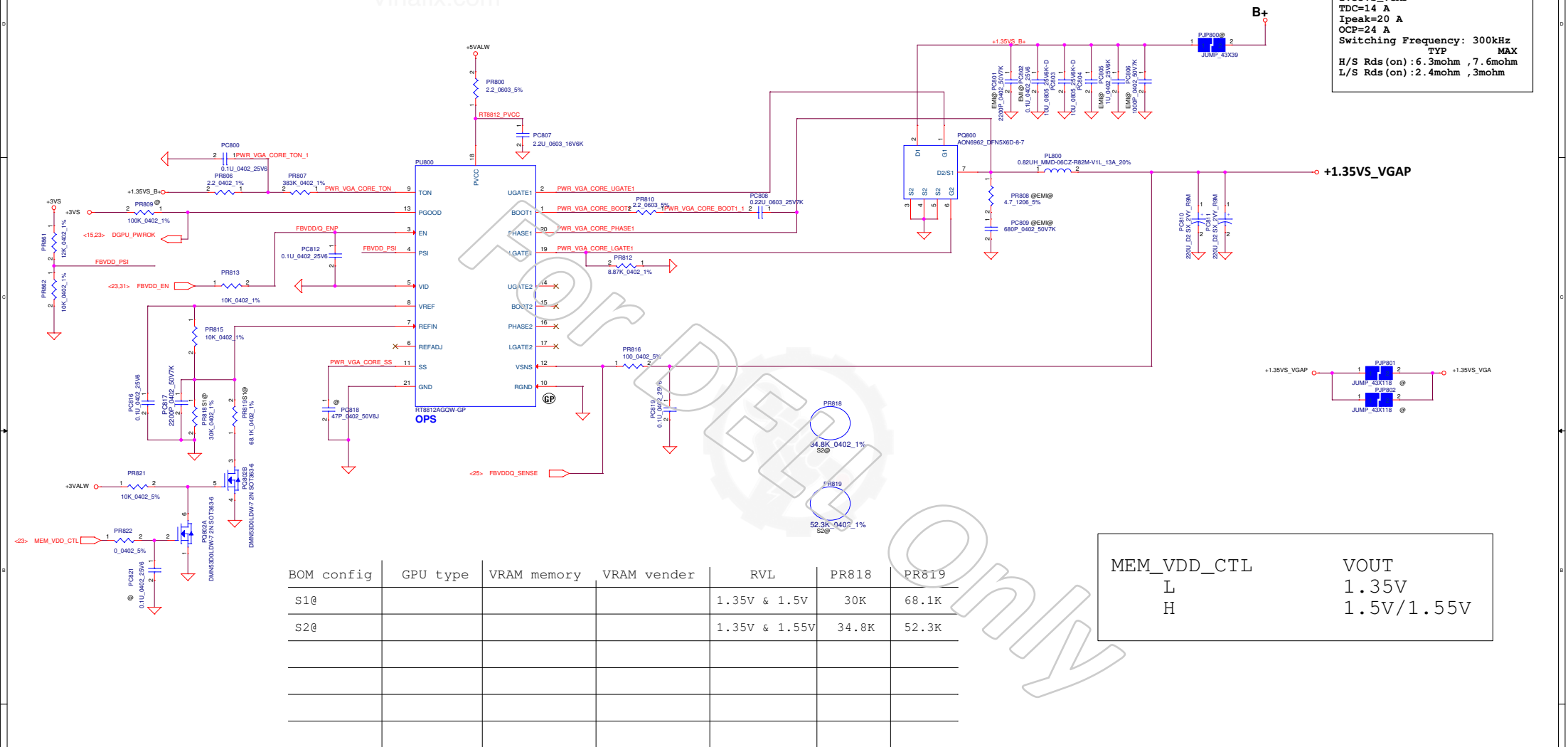
+NVVDD1
 TDC 50A
 Peak Current 106A
 OCP=127.2A
 Fsw=305KHz
 DCR:0.98mohm +-5%
 TYP MAX
 H/S Rds(on):6.8mohm ,8.6mohm
 L/S Rds(on):2mohm ,2.5mohm

N17P_G1	VDD	VDD5
TDC	50	12.6
Peak	106	18



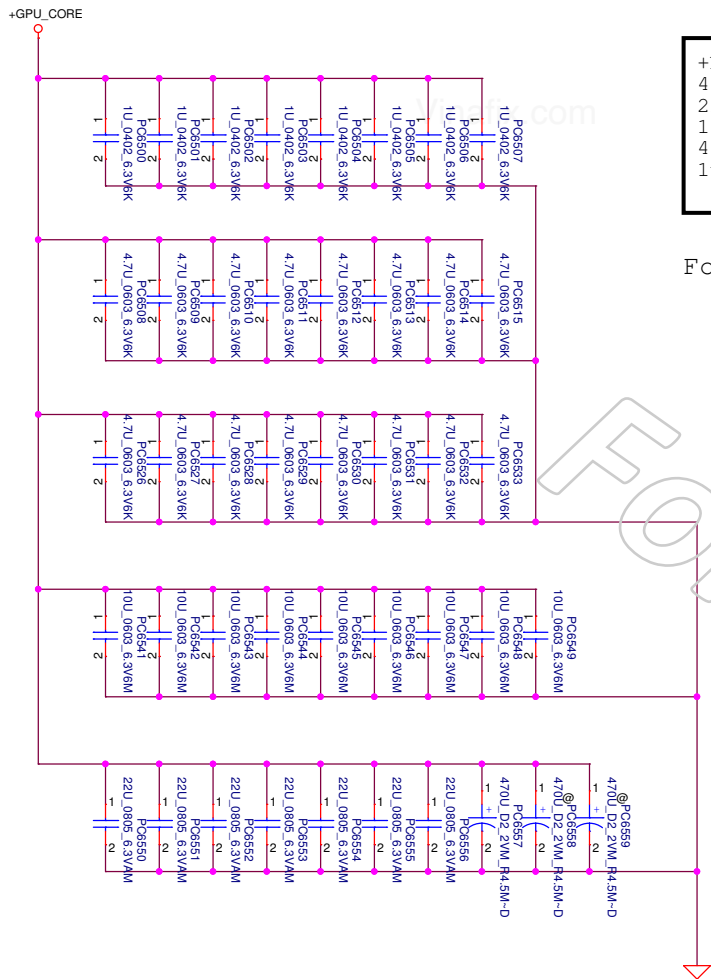
	1Phase DEM	1Phase CCM
PSI	0V	0.8V
PR6229	NC	NC
PR6228	215Kohm	115Kohm
PR6230	0ohm	100Kohm

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/09/18	Deciphered Date	2016/09/18	Title	PWR+NVVDD2	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev 1 (4/00)
				LA-E993P		
Date: Tuesday, March 05, 2018				Sheet	66	of 78



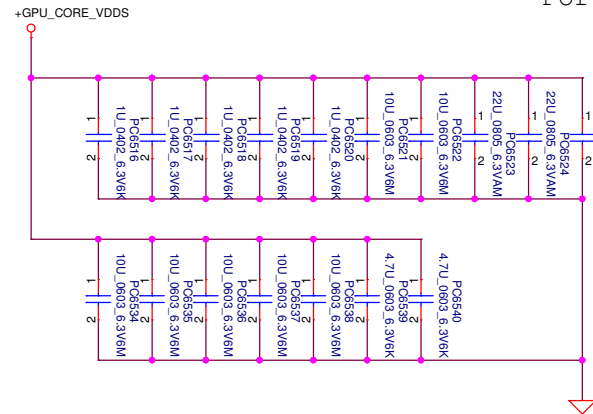
BOM config	GPU type	VRAM memory	VRAM vender	RVL	PR818	PR819
s1e				1.35V & 1.5V	30K	68.1K
s2e				1.35V & 1.55V	34.8K	52.3K

MEM_VDD_CTL	VOUT
L	1.35V
H	1.5V/1.55V



+NVVDD
 470uF X 1
 22uF_0805 X 7
 10uF_0603 X 9
 4.7uF_0603 X 16
 1uF_0402 X 8

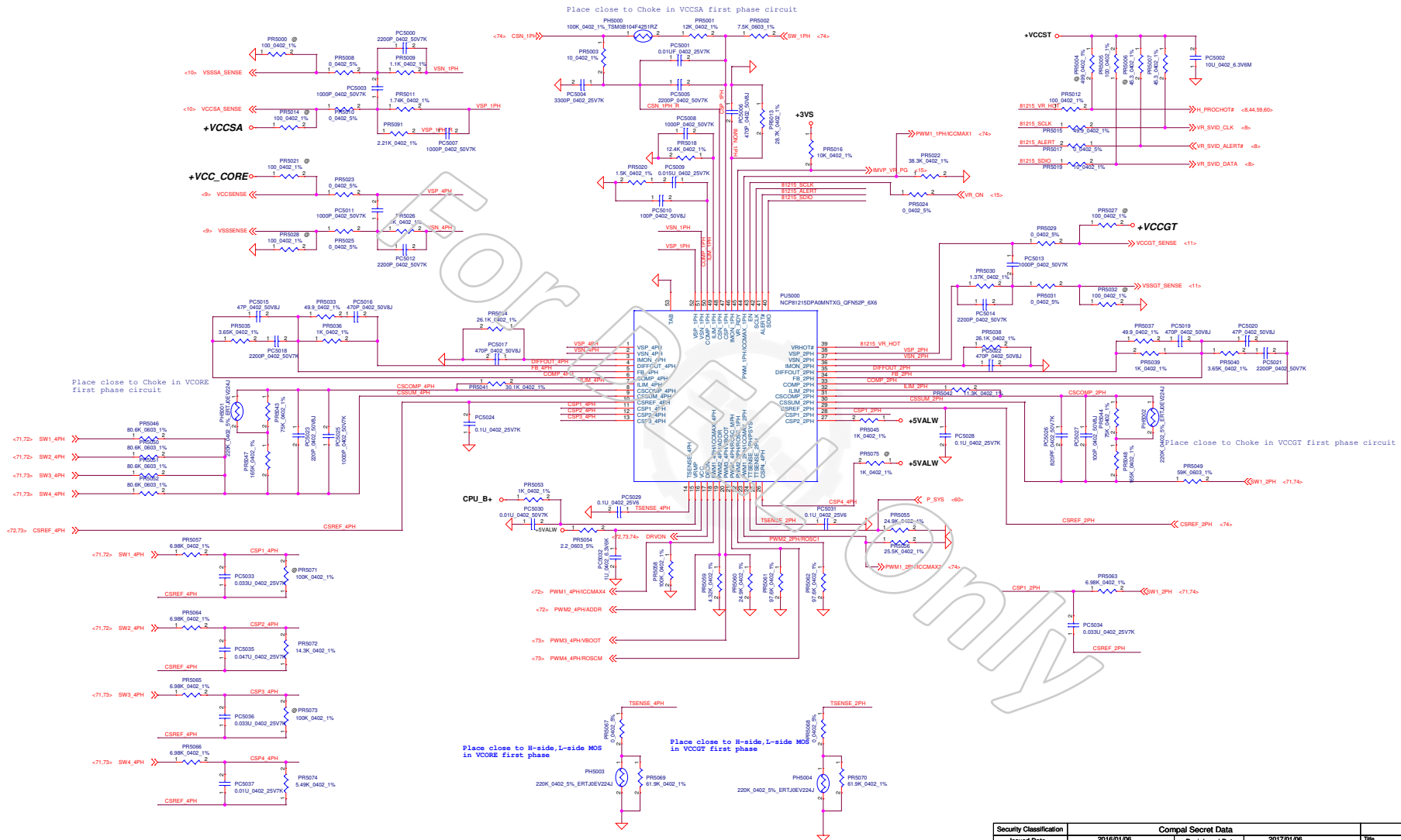
For NV N17P latest spec



+NVVDD
 22uF_0805 X 3
 10uF_0603 X 7
 4.7uF_0603 X 2
 1uF_0402 X 5

For NV N17P latest spec

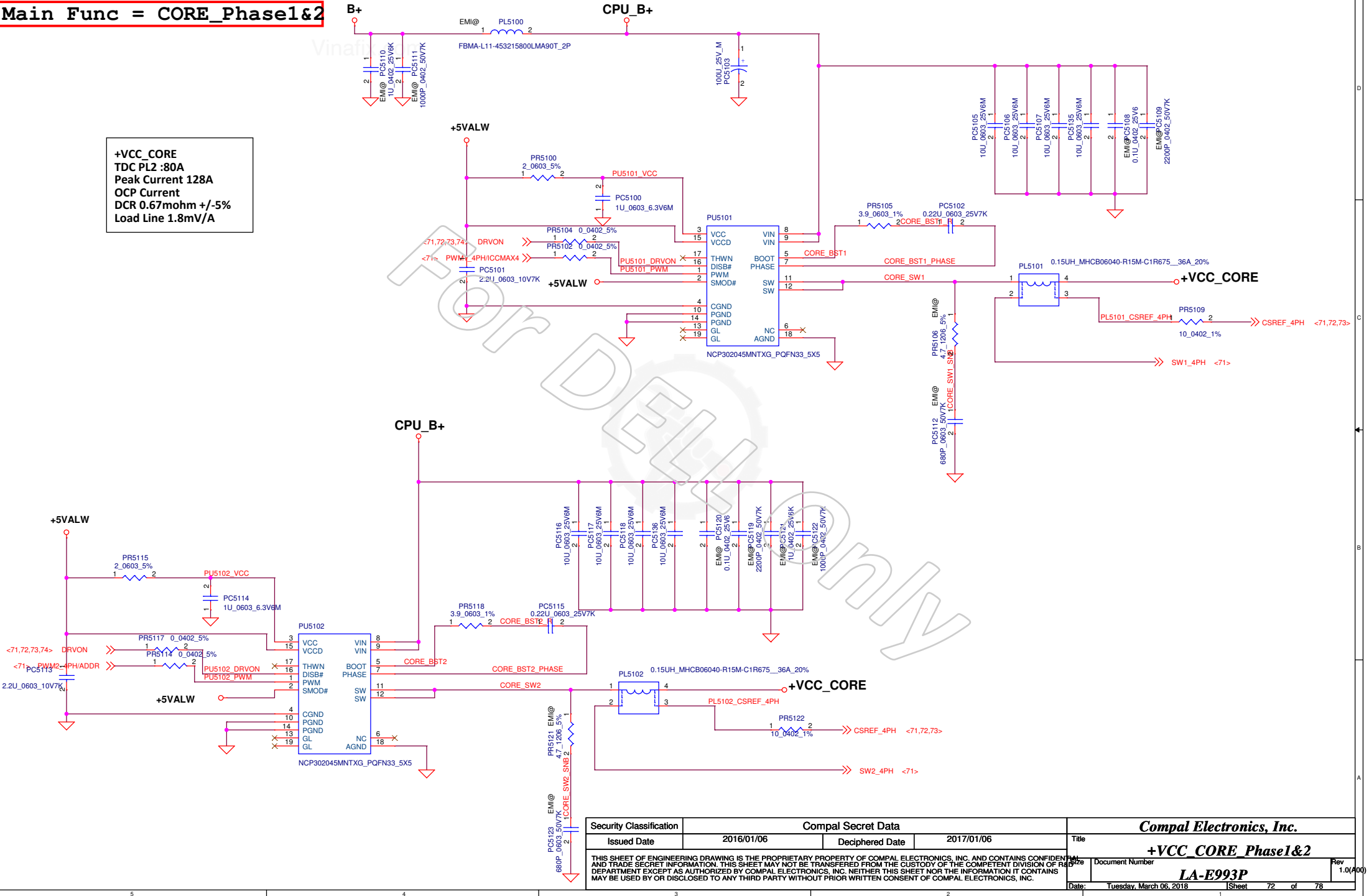
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/09/18	Deciphered Date	2016/09/18	Title	VGA DECOUPLING
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-E993P
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Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/08	Designed Date	2017/01/08	File
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PWR VCORE NCP81215				Rev
LA-E993P				1 of 1
Tuesday, March 08, 2017				Page

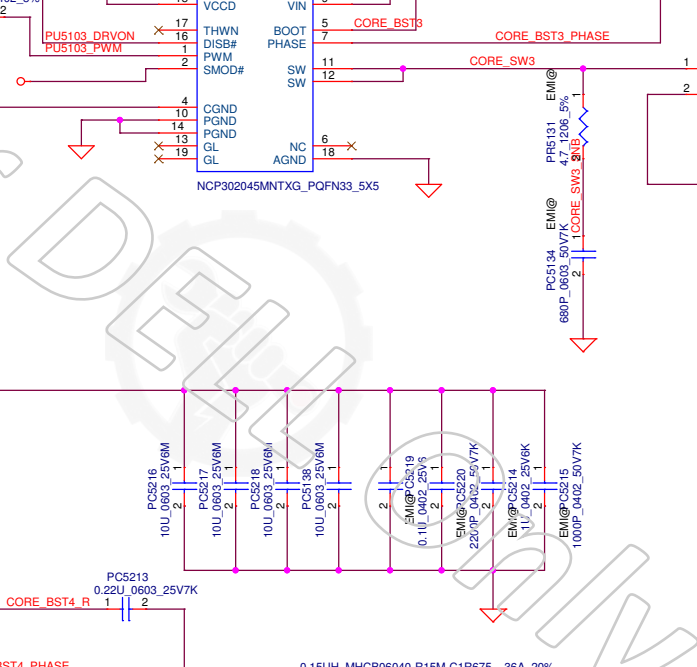
Main Func = CORE_Phase1&2

+VCC_CORE
TDC PL2 :80A
Peak Current 128A
OCP Current
DCR 0.67mohm +/-5%
Load Line 1.8mV/A



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2016/01/06		Title	
		Deciphered Date		+VCC CORE Phase1&2	
				Document Number	
				LA-E993P	
				Date	
				Tuesday, March 06, 2018	
				Sheet	
				72 of 78	

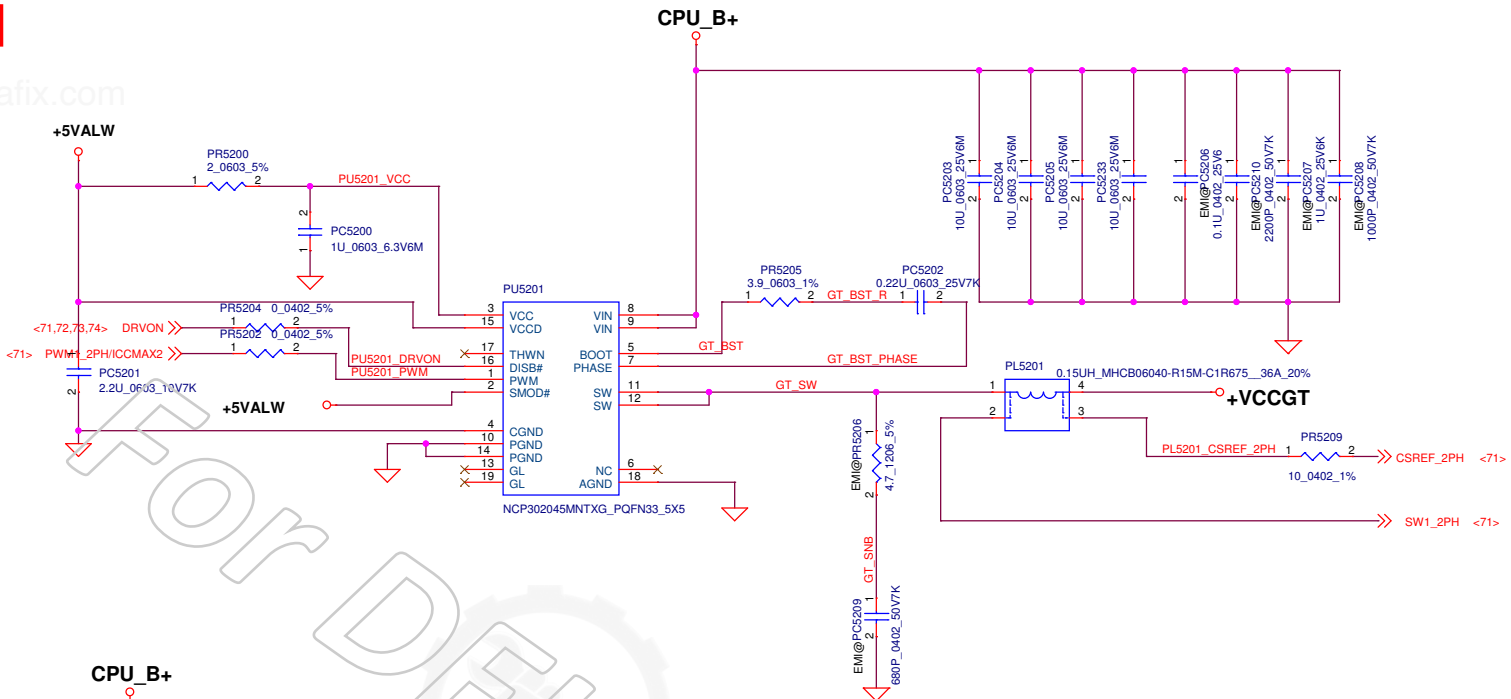
4



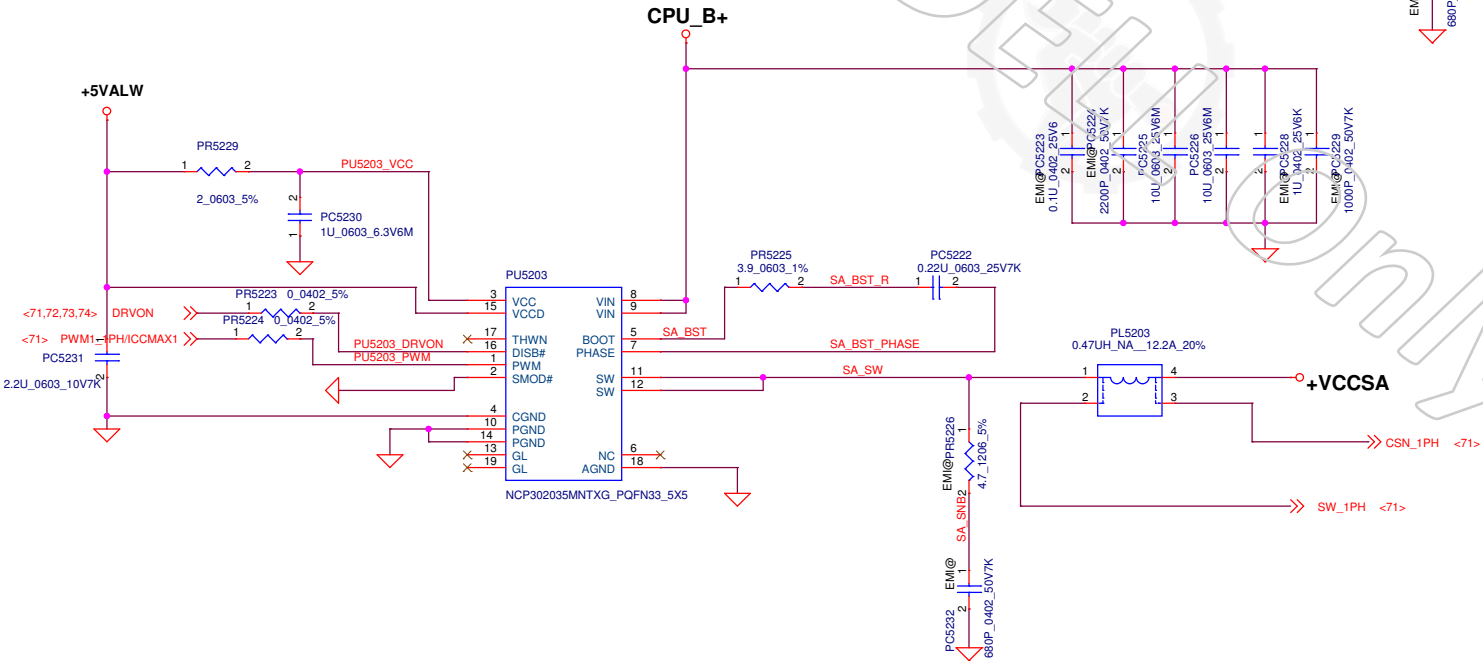
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Main Func = VCC_GT/+VCC_SA

+VCCGT
TDC PL2 :22.4A
Peak Current 32A
DCR 0.9mohm +/-5%
Load Line 2.7mV/A



+VCCSA
TDC PL2 :7.77A
Peak Current 11.1A
DCR 6.2mohm +/-5%
Load Line 10.3mV/A



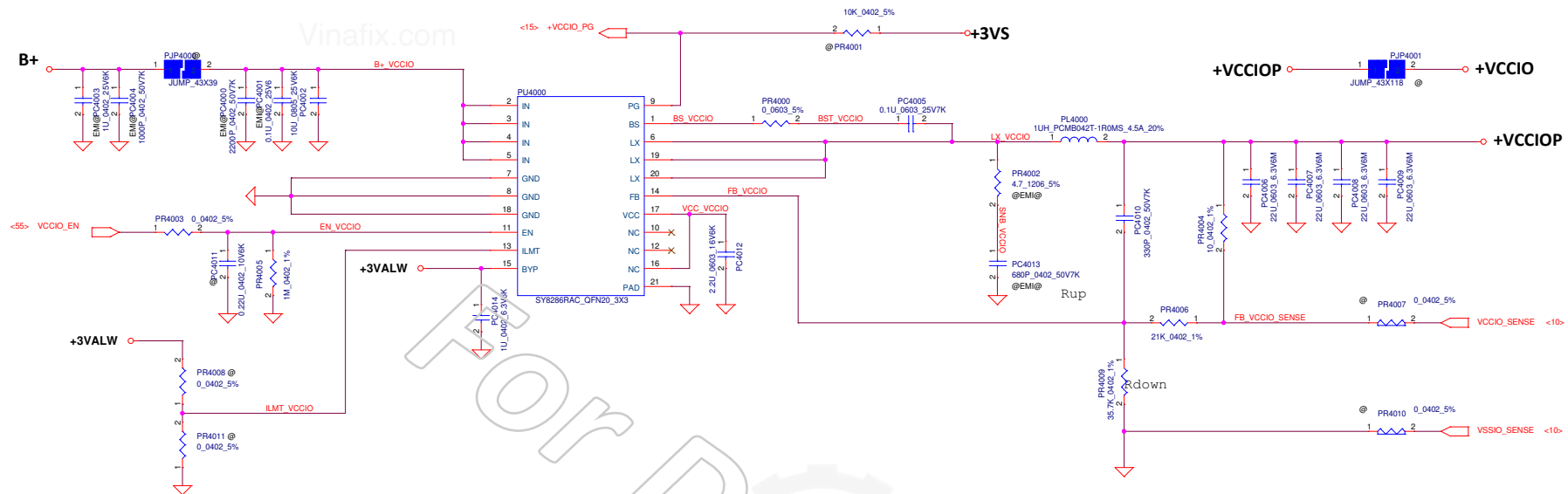
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
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+VCC_CORE
220uF*2
330uF*1
47uF*2
22uF*31
10uF*21
1uF*48

+VCCGT
220uF*2
22uF*26
10uF*10
1uF*12

+VCCSA
47uF*4
22uF*2
10uF*7
1uF*1

Input Current:0.417A
 $0.95 \times 3.85 / 0.85 / 12V = 0.417A$



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

+VCCIOP (0.95V)
TDC 4.48 A
Peak Current 6.4 A
OCP Current 9 A
FSW:500KHz

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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	NOTE
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	NOTE
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